



P565A4-LM2

(AM4 Turpan)

(PCB2)

V0.3

ECS
CONFIDENTIAL

SCHEMATICS TABLE:

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18	FCH PCIe/SATA/GPIO	44	+1V2_DIMM/+DDR_VTT/2V5_DIMM
19	FCH USB/CLOCK	45	+1V8_S5/+1V8_S0/+VDDP_S0
20	FCH POWER	46	+VDD_FCH/+VDDP_S5
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AM4 Processor

Processor Features	Socket AM4 Processor						
	Type 0	Type 1	Type 2	Type 3 ³	Type 4	Type 5	Type 6
Family/Model Numbers ¹	Family 15h, Models 60h-6Fh	Family 17h, Models 20h-2Fh	Family 17h, Models 00h-0Fh	Family 17h, Models 10h-1Fh	Family 17h, Models 70h-7Fh	Family 17h, Models 60h-6Fh	Family 19h, Models 20h-2Fh
On-chip Graphics	3 Display Engines, 3 DDI Ports	3 Display Engines, 2 DDI Ports ²	N/A	4 Display Engines, 3 DDI Ports ³	N/A	4 Display Engines, 3 DDI Ports	N/A
Memory	Two DDR4 Channels	Two DDR4 Channels	Two DDR4 Channels	Two DDR4 Channels	Two DDR4 Channels	Two DDR4 Channels	Two DDR4 Channels
	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total	DDR4 SO-DIMMs or DDR4 UDIMMs One or Two per channel, up to Four Total
PCIe ^{3, 4}	P_GFX x8 P_GPP x6	P_GFX x4 P_GPP x4	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x8 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2
SATA	SATA x2	SATA x2	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)
USB Ports	USB2 x4 USB3 x4	USB2 x4 USB3 x4	USB2 x4 USB3 x4	USB2 x4 USB3 x4	USB2 x4 USB3 x4	USB2 x4 USB3 x4	USB2 x4 USB3 x4

AMD 500 Series chipset

Engineering Name	USB			SATA 3.0 Ports	Chipset General Purpose PCIe® Gen 3	Chipset General Purpose I/O	AM4 Processor GFX PCIe® Interface	AM4 Processor Overclocking Enabled	Chipset Package	Chipset TDP	NVMe and SATA RAID2
	3.2 G2 (10 Gbps)	3.2 G1 (5 Gbps)	2.0								
CS2019.A	2	1	6	2 + 2 ¹	4 + 2 ¹	8	1 x 16	No	LFBGA	See Table 29 on page 40.	0/1/10
CS2019.C	2	2	6	4 + 2 ¹	8 + 2 ¹	8	1x16 / 2x8	Yes	LFBGA		0/1/10
CS2019.D	2	2	6	4 + 2 ¹	8 + 2 ¹	8	1x16 / 2x8	No	LFBGA		0/1/10

專案RD	
HW	Vic Tsao
Power	Jacky Hsieh
BIOS	Armi Hsu
AMD 參考資料(附上版本日期)	
PDG	50724_AM4_MBDG_AGILE_rev_1_22_v02 (September 2019)
EDS	56316_0.54_EDS (August 2019)
CRB	Artic RevB Schematic (July 2019)
Code & ID	
Model Code	
Project Code	
LAN	SVID : 17AA / SSID :
Audio	SVID : 17AA / SSID :

	Clientele	PCB Size
V0.1	LENOVO	267*245
V0.2	LENOVO	267*245
V1.0	LENOVO	267*245

PSU 12 V2 Capability Recommendations		
Processor TDP	Continuous Current	Peak Current
165 W	37.5 A	40 A
95 W	22 A	29 A
65 W	21 A	28 A
35 W	13 A	16.5 A

12-16A support for 2x2 (4pin) connector

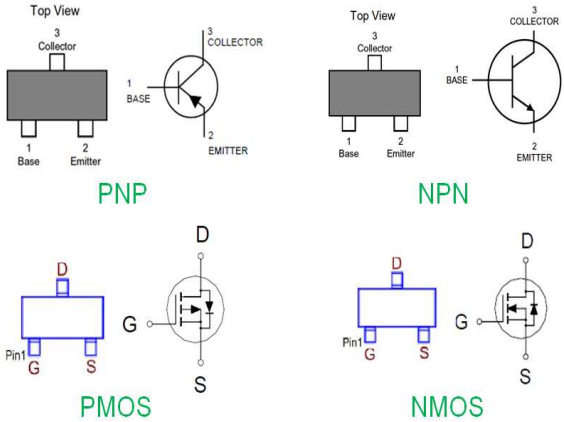
18-24A support for 2x3 (6pin) connector

24-32A support for 2x4 (8pin) connector

Model Version	AGPIO18	AGPIO89	EGPIO42	EGPIO119	AGPIO21	AGPIO88	SVID/SSID
Think M75s-2	X	X	X	0	1	0	17AA/3197
Think M75s-2A	X	X	X	1	1	0	17AA/318E
QT M540-1	X	X	X	0	0	1	17AA/318F
QT M540-2	X	X	X	1	0	1	17AA/3198
Consumer T550	X	X	X	0	0	0	17AA/3728

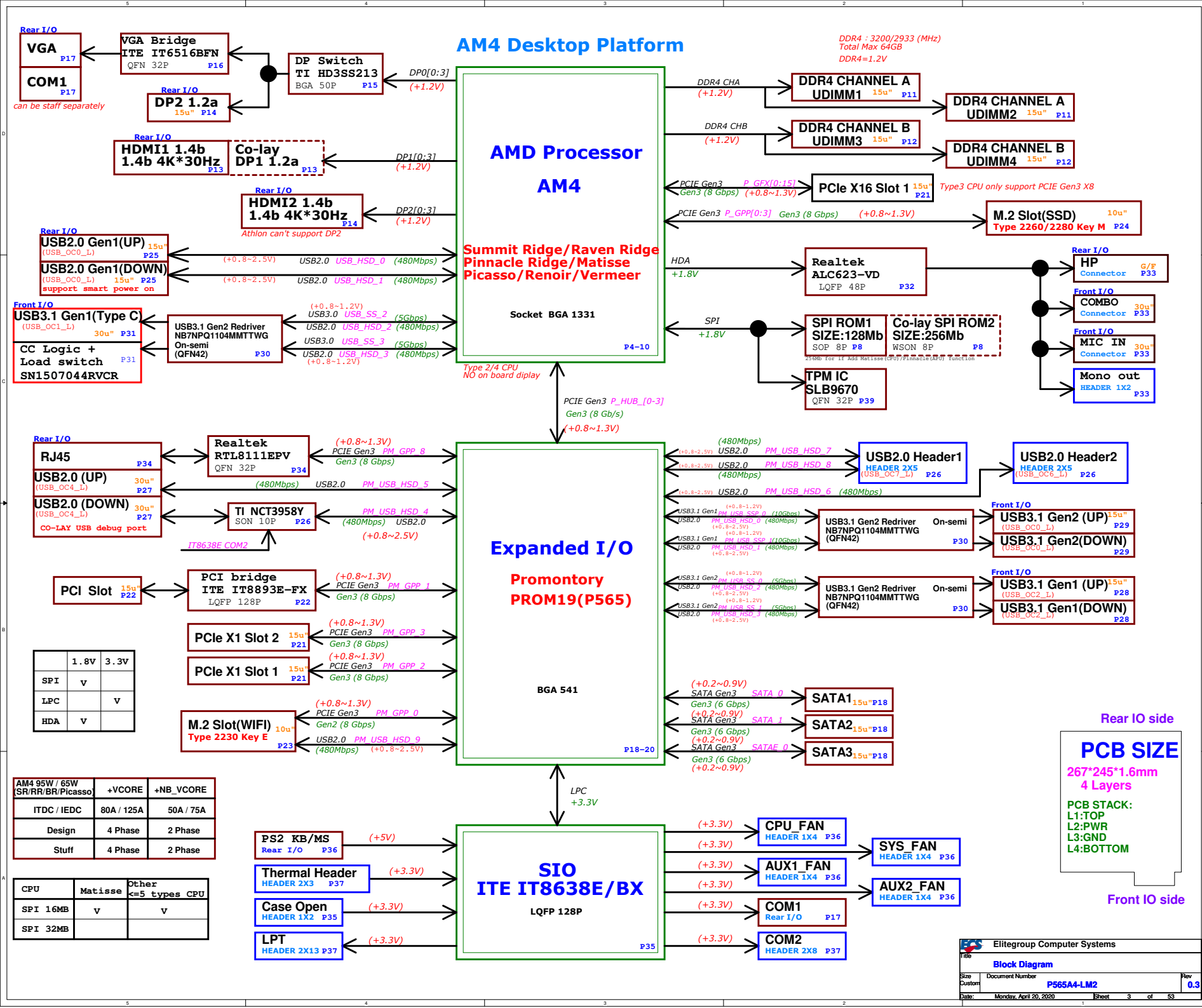
Socket AM4 processor						
Features	Raven Ridge(Raven-2) (Family 17h,00h-0Fh)	Summit Ridge Pinnacle Ridge (Family 17h,10h-1Fh)	Raven Ridge (Raven-1) Picasso (Family 17h,10h-1Fh)	Matisse (Family 17h,70h-7Fh)	Renior (Family 17h,60h-6Fh)	Vermeer (Family 17h,20h-2Fh)
	Type1 (cost down ver.)	Type 2	Type 3	Type 4	Type 5	Type 6
on-chip Graphics	3 Display Engines 2 DDI Ports	NA	4 Display Engines 3 DDI Ports	NA	4 Display Engines 3 DDI Ports	NA
PCIe	P_GFX x4 P_GPP x4	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x8 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2	P_GFX x16 P_GPP x8 or P_GPP x6 and SATA x2
SATA	SATA x2	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)	SATA x2 (if two P_GPP are not used)
USB	USB2 x4 USB3 Gen1 x4	USB2 x4 USB3 Gen1 x4	USB2 x4 USB3 Gen1 x4	USB2 x4 USB3 Gen1 x4	USB2 x4 USB3 Gen1 x4	USB2 x4 USB3 Gen1 x4

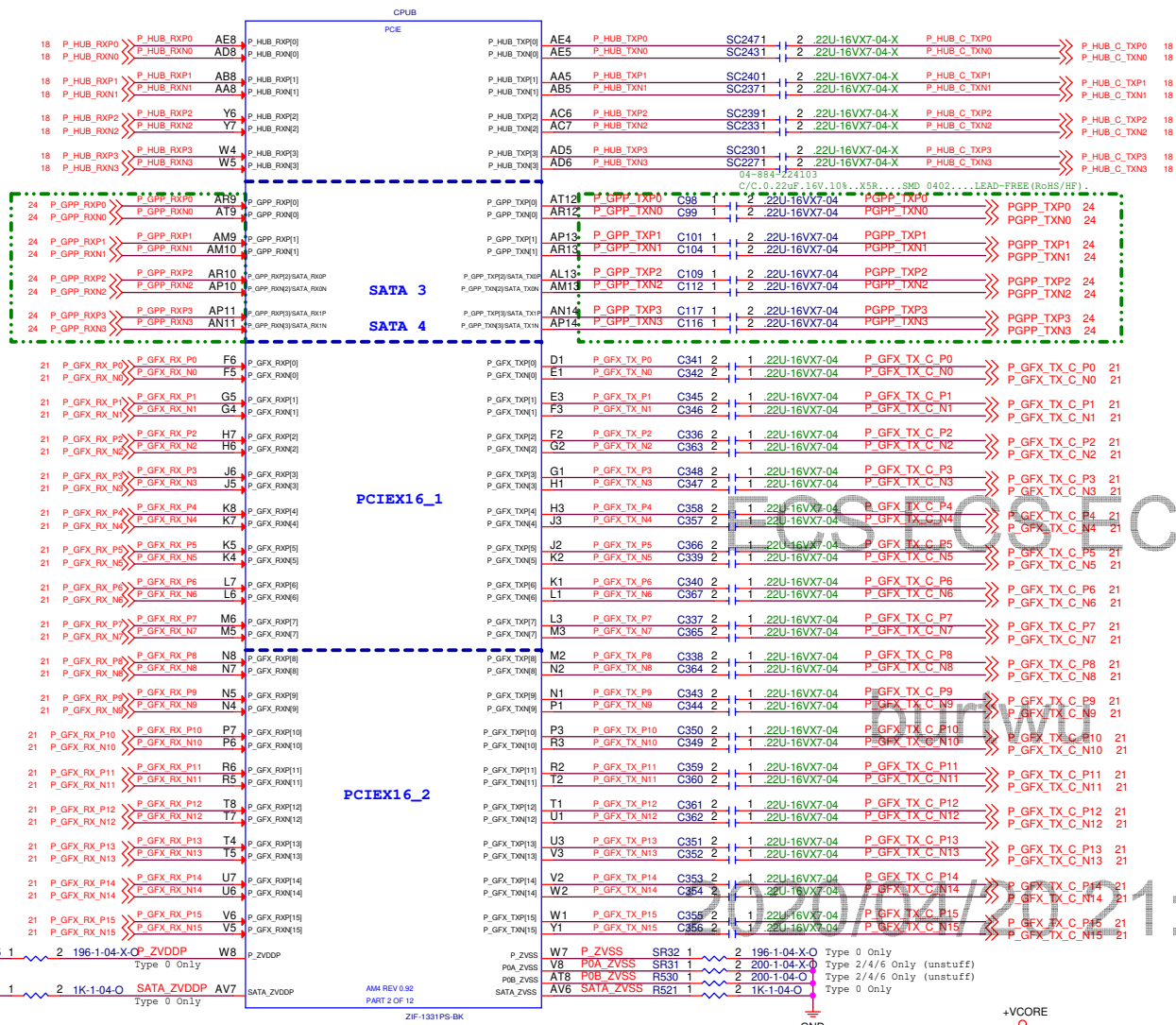
Power Rail Request	Bristol Ridge(65W)	Summit Ridge(65W/95W)	Raven Ridge(65W)	Pinnacle Ridge Matisse(105W)	Superset (SR&RR&BR&PR)	Superset (BR&SR&RR&PR)
VCORE	TDC=65A,EDC=95A 3 Phase / Dual MOS *3	TDC=80A,EDC=125A 4 Phase / Dual MOS *4	TDC=65A,EDC=95A 3 Phase / Dual MOS *3	TDC=95A,EDC=140A 4 Phase / Dual MOS *4	TDC=95A,EDC=140A 4 Phase / Dual MOS *4	TDC=95A,EDC=140A 4 Phase / Dual MOS *4
VDDNB	TDC=50A,EDC=75A 2 Phase / H*2 L*2 MOS	TDC=30A,EDC=35A 2 Phase / H*1 L*1 MOS	TDC=50A,EDC=75A 2 Phase / H*2 L*2 MOS	TDC=50A,EDC=75A 2 Phase / H*2 L*2 MOS	TDC=50A,EDC=75A 2 Phase / H*2 L*2 MOS	TDC=50A,EDC=75A 2 Phase / H*2 L*2 MOS
VDDP_S0	+1.05V	N/A	+0.9V	+0.9V	+0.9V/+1.05V	Stuff for CORETYPE1 select
VDDP_S5	+1.05V	+0.9V	+0.9V	+0.9V	+0.9V/+1.05V	Stuff for CORETYPE1 select
VDDCR_SOC_S5	S3/4/5: 0.775V S0: track +NB_VCORE	N/A	N/A	N/A	N/A	Stuff for CORETYPE1 select



Promontory Chipset	
Feature	PROM19D(P565)
USB3.1 Gen2	USB_SSP Port0~1
USB3.1 Gen1	USB_SS Port 0~1
USB2.0	USB_HSD Port0~9
SATA 3.0	SATA port0~3
PCI Express Gen3 GPP	GPP lane0~1 GPP lane4~7 GPP lane8~9
PCI Express CLK	CLK0~9

Elitegroup Computer Systems		
Information		
File	Document Number	Rev
	P565A4-LM2	0.3
Date:	Monday, April 20, 2020	Sheet 2 of 53





20200205 V0.1 to V0.2 Vic
[Follow CRB] M.2 SSD signal
change from P565 to CPU

M.2 SSD

To PCIe16 Slot 1

Features	Pinnacle Ridge (Family 17h,00h-0Fh)	Raven Ridge(Raven-2) (Family 17h,20h-2Fh)
PCIe	P_HUB [0-3] P_GFX [0-15] P_GPP [0-1] P_GPP [2-3]	P_HUB [0-1] P_GFX [0-3] P_GPP [0-1]
SATA	SATA [0-1] (if P_GPP [2-3] are not used)	SATA [0-1]

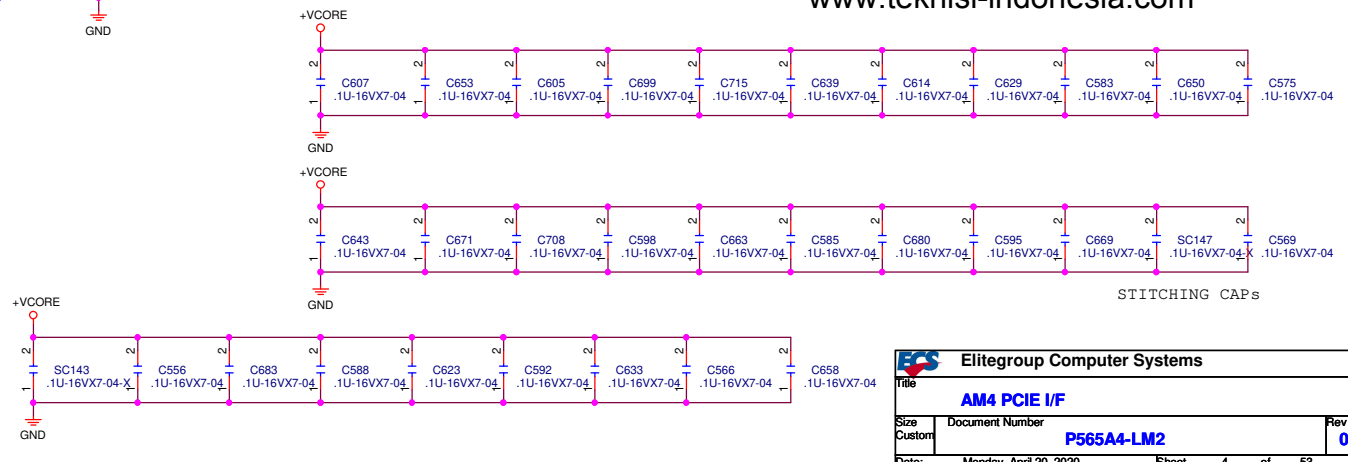
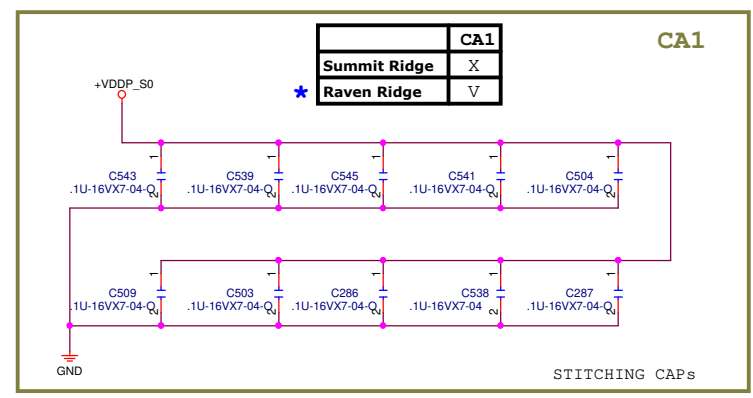
Features	Raven Ridge(Raven-1)/Picasso (Family 17h,10h-1Fh)	Matisse (Family 17h,70h-7Fh)
PCIe	P_HUB [0-3] P_GFX [0-7] P_GPP [0-1] P_GPP [2-3]	P_HUB [0-3] P_GFX [0-15] P_GPP [0-1] P_GPP [2-3]
SATA	SATA [0-1] (if P_GPP [2-3] are not used)	SATA [0-1] (if P_GPP [2-3] are not used)

Features	Renior (Family 17h,60h-6Fh)	Vermeer (Family 17h,20h-2Fh)
PCIe	P_HUB [0-3] P_GFX [0-15] P_GPP [0-1] P_GPP [2-3]	P_HUB [0-3] P_GFX [0-15] P_GPP [0-1] P_GPP [2-3]
SATA	SATA [0-1] (if P_GPP [2-3] are not used)	SATA [0-1] (if P_GPP [2-3] are not used)

Table 37. Component Table—PCIe[®] Interface to Connector or Onboard Device

Ref	Value ^{1,2}	Tolerance	Package	Placement Location
C _{Coupling}	PCIe [®]	10%	(0402)	Place as pairs ^{3,4}
<ul style="list-style-type: none">Gen4 Allowable Range: 176 to 265 nF Recommended Value: 220 nFGen3 Allowable Range: 176 to 265 nF Recommended Value: 220 nFGen2 Allowable Range: 75 to 200 nF Recommended Value: 100 nF				
<p>Note: 1. Capacitor material is XSR. 2. When Gen2, Gen3, and Gen4 devices are supported, use 220 nF. 3. Placing capacitors as pairs requires traces to be length matched. 4. Place the AC-coupling capacitors for each pair as a pair within 0.889 mm of each other. See PCIe AC-Coupling Capacitors for more details.</p>				

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DDR4 CH.A

11	M_DM_A[0..8]	<<	M_DM_A[0..8]
11	M_DATA_A[0..63]	<<	M_DATA_A[0..63]
11	M_CLK_A_P[0..3]	<<	M_CLK_A_P[0..3]
11	M_CLK_A_N[0..3]	<<	M_CLK_A_N[0..3]
11	M_CKE_A[0..3]	<<	M_CKE_A[0..3]
11	M_CS_A_L[0..3]	<<	M_CS_A_L[0..3]
11	M_ODT_A[0..3]	<<	M_ODT_A[0..3]
11	M_BS_A[0..1]	<<	M_BS_A[0..1]
11	M_BS_A[0..1]	<<	M_BS_A[0..1]
11	M_BG_A[0..1]	<<	M_BG_A[0..1]
11	M_MA_A[0..17]	<<	M_MA_A[0..17]
11	M_DQS_A_P[0..8]	<<	M_DQS_A_P[0..8]
11	M_DQS_A_N[0..8]	<<	M_DQS_A_N[0..8]
11	M_ACT_A_N	<<	M_ACT_A_N
11	M_PARITY_A	<<	M_PARITY_A
11	M_ALERT_A_L	<<	M_ALERT_A_L
11	M_DRAMRST_A_L	<<	M_DRAMRST_A_L
11	M_EVENT_A_L	<<	M_EVENT_A_L
11	M_DATA_A_CB[0..7]	<<	M_DATA_A_CB[0..7]

DDR4 CH.B

12	M_DM_B[0..8]	<<	M_DM_B[0..8]
12	M_DATA_B[0..63]	<<	M_DATA_B[0..63]
12	M_CLK_B_P[0..3]	<<	M_CLK_B_P[0..3]
12	M_CLK_B_N[0..3]	<<	M_CLK_B_N[0..3]
12	M_CKE_B[0..3]	<<	M_CKE_B[0..3]
12	M_CS_B_L[0..3]	<<	M_CS_B_L[0..3]
12	M_ODT_B[0..3]	<<	M_ODT_B[0..3]
12	M_BS_B[0..1]	<<	M_BS_B[0..1]
12	M_BS_B[0..1]	<<	M_BS_B[0..1]
12	M_BG_B[0..1]	<<	M_BG_B[0..1]
12	M_MA_B[0..17]	<<	M_MA_B[0..17]
12	M_DQS_B_P[0..8]	<<	M_DQS_B_P[0..8]
12	M_DQS_B_N[0..8]	<<	M_DQS_B_N[0..8]
12	M_ACT_B_N	<<	M_ACT_B_N
12	M_PARITY_B	<<	M_PARITY_B
12	M_ALERT_B_L	<<	M_ALERT_B_L
12	M_DRAMRST_B_L	<<	M_DRAMRST_B_L
12	M_EVENT_B_L	<<	M_EVENT_B_L
12	M_DATA_B_CB[0..7]	<<	M_DATA_B_CB[0..7]

M_MA_A0	AA32	MA_ADD[0]
M_MA_A1	T32	MA_ADD[1]
M_MA_A2	T35	MA_ADD[2]
M_MA_A3	T31	MA_ADD[3]
M_MA_A4	R30	MA_ADD[4]
M_MA_A5	R33	MA_ADD[5]
M_MA_A6	R32	MA_ADD[6]
M_MA_A7	P34	MA_ADD[7]
M_MA_A8	P30	MA_ADD[8]
M_MA_A9	P31	MA_ADD[9]
M_MA_A10	AA36	MA_ADD[10]
M_MA_A11	P33	MA_ADD[11]
M_MA_A12	N35	MA_ADD[12]
M_MA_A13	AE32	MA_ADD[13]
M_ACT_A_N	M35	MA_ACT_L
M_BG_A0	N31	MA_BG[0]
M_BG_A1	N32	MA_BG[1]
M_BS_A0	AA35	MA_BANK[0]
M_BS_A1	AA33	MA_BANK[1]
M_DM_A0	K19	MA_DM[0]
M_DM_A1	J23	MA_DM[1]
M_DM_A2	G26	MA_DM[2]
M_DM_A3	H30	MA_DM[3]
M_DM_A4	AJ31	MA_DM[4]
M_DM_A5	AM31	MA_DM[5]
M_DM_A6	AL29	MA_DM[6]
M_DM_A7	AL26	MA_DM[7]
M_DM_A8	G34	MA_DM[8]
M_DQS_A_P0	H19	MA_DQS_H[0]
M_DQS_A_N0	G19	MA_DQS_L[0]
M_DQS_A_P1	F23	MA_DQS_L[1]
M_DQS_A_N1	G23	MA_DQS_L[1]
M_DQS_A_P2	F27	MA_DQS_L[2]
M_DQS_A_N2	F26	MA_DQS_L[2]
M_DQS_A_P3	F30	MA_DQS_L[3]
M_DQS_A_N3	E30	MA_DQS_L[3]
M_DQS_A_P4	AJ33	MA_DQS_L[4]
M_DQS_A_N4	AJ34	MA_DQS_L[4]
M_DQS_A_P5	AN32	MA_DQS_L[5]
M_DQS_A_N5	AN33	MA_DQS_L[5]
M_DQS_A_P6	AP29	MA_DQS_L[6]
M_DQS_A_N6	AN29	MA_DQS_L[6]
M_DQS_A_P7	AP26	MA_DQS_L[7]
M_DQS_A_N7	AN26	MA_DQS_L[7]
M_DQS_A_P8	H34	MA_DQS_L[8]
M_DQS_A_N8	H33	MA_DQS_L[8]
M_CLK_A_P0	T34	MA_CLK_H[0]
M_CLK_A_N0	U34	MA_CLK_L[0]
M_CLK_A_P1	U33	MA_CLK_H[1]
M_CLK_A_N1	V33	MA_CLK_L[1]
M_CLK_A_P2	V35	MA_CLK_H[2]
M_CLK_A_N2	V36	MA_CLK_L[2]
M_CLK_A_P3	V32	MA_CLK_H[3]
M_CLK_A_N3	W32	MA_CLK_L[3]
M_DRAMRST_A_L	L33	MA_RESET_L
M_EVENT_A_L	LW35	MA_EVENT_L
M_CKE_A0	M32	MAO_CKE[0]
M_CKE_A1	M30	MAO_CKE[1]
M_CKE_A2	M33	MAO_CKE[2]
M_CKE_A3	L34	MAO_CKE[3]
M_ODT_A0	AD35	MAO_ODT[0]
M_ODT_A1	AF31	MAO_ODT[1]
M_ODT_A2	AD33	MAO_ODT[2]
M_ODT_A3	AF34	MAO_ODT[3]
M_CS_A_L0	AC33	MAO_CS_L[0]
M_CS_A_L1	AE35	MAO_CS_L[1]
M_CS_A_L2	AC34	MAO_CS_L[2]
M_CS_A_L3	AE34	MAO_CS_L[3]
M_MA_A17	AF33	MA_ADD_17
M_MA_A16	AB34	MA_RAS_L_ADD[16]
M_MA_A15	AB32	MA_CAS_L_ADD[15]
M_MA_A14	AB35	MA_WE_L_ADD[14]
M_ALERT_A_L	N34	MA_ALERT_L
M_PARITY_A	Y33	MA_PAROUT

AMA REV 0.92

PART 1 OF 12

AMA

MA_DATA[0]	E18	M_DATA_A0
MA_DATA[1]	J18	M_DATA_A1
MA_DATA[2]	U20	M_DATA_A2
MA_DATA[3]	H21	M_DATA_A3
MA_DATA[4]	H18	M_DATA_A4
MA_DATA[5]	F18	M_DATA_A5
MA_DATA[6]	G20	M_DATA_A6
MA_DATA[7]	F20	M_DATA_A7
MA_DATA[8]	H22	M_DATA_A8
MA_DATA[9]	G22	M_DATA_A9
MA_DATA[10]	E24	M_DATA_A10
MA_DATA[11]	J24	M_DATA_A11
MA_DATA[12]	F21	M_DATA_A12
MA_DATA[13]	J21	M_DATA_A13
MA_DATA[14]	H24	M_DATA_A14
MA_DATA[15]	F24	M_DATA_A15
MA_DATA[16]	J26	M_DATA_A16
MA_DATA[17]	J27	M_DATA_A17
MA_DATA[18]	G28	M_DATA_A18
MA_DATA[19]	H28	M_DATA_A19
MA_DATA[20]	H25	M_DATA_A20
MA_DATA[21]	G25	M_DATA_A21
MA_DATA[22]	E28	M_DATA_A22
MA_DATA[23]	H27	M_DATA_A23
MA_DATA[24]	F29	M_DATA_A24
MA_DATA[25]	J30	M_DATA_A25
MA_DATA[26]	H31	M_DATA_A26
MA_DATA[27]	F32	M_DATA_A27
MA_DATA[28]	J29	M_DATA_A28
MA_DATA[29]	G29	M_DATA_A29
MA_DATA[30]	E31	M_DATA_A30
MA_DATA[31]	G31	M_DATA_A31
MA_DATA[32]	AH34	M_DATA_A32
MA_DATA[33]	AJ30	M_DATA_A33
MA_DATA[34]	AK30	M_DATA_A34
MA_DATA[35]	AL34	M_DATA_A35
MA_DATA[36]	AL31	M_DATA_A36
MA_DATA[37]	AH32	M_DATA_A37
MA_DATA[38]	AK33	M_DATA_A38
MA_DATA[39]	AK32	M_DATA_A39
MA_DATA[40]	AM34	M_DATA_A40
MA_DATA[41]	AM33	M_DATA_A41
MA_DATA[42]	AP31	M_DATA_A42
MA_DATA[43]	AR33	M_DATA_A43
MA_DATA[44]	AL32	M_DATA_A44
MA_DATA[45]	AL31	M_DATA_A45
MA_DATA[46]	AF34	M_DATA_A46
MA_DATA[47]	AF32	M_DATA_A47
MA_DATA[48]	AR31	M_DATA_A48
MA_DATA[49]	AK29	M_DATA_A49
MA_DATA[50]	AM28	M_DATA_A50
MA_DATA[51]	AL28	M_DATA_A51
MA_DATA[52]	AM30	M_DATA_A52
MA_DATA[53]	AN30	M_DATA_A53
MA_DATA[54]	AP28	M_DATA_A54
MA_DATA[55]	AR28	M_DATA_A55
MA_DATA[56]	AK27	M_DATA_A56
MA_DATA[57]	AK26	M_DATA_A57
MA_DATA[58]	AP25	M_DATA_A58
MA_DATA[59]	AR25	M_DATA_A59
MA_DATA[60]	AN27	M_DATA_A60
MA_DATA[61]	AL26	M_DATA_A61
MA_DATA[62]	AM25	M_DATA_A62
MA_DATA[63]	AM25	M_DATA_A63
MA_CHECK[0]	F33	M_DATA_A_CB0
MA_CHECK[1]	G32	M_DATA_A_CB1
MA_CHECK[2]	K31	M_DATA_A_CB2
MA_CHECK[3]	K32	M_DATA_A_CB3
MA_CHECK[4]	E33	M_DATA_A_CB4
MA_CHECK[5]	E34	M_DATA_A_CB5
MA_CHECK[6]	J32	M_DATA_A_CB6
MA_CHECK[7]	J33	M_DATA_A_CB7
MA_ZVDDIO_MEM_S3	Y34	MA_ZVDDIO
MA_ZVSS	AJ37	MA_ZVSS

Type 0 Only
R622 1 2 39 2-1-04-0
R576 1 2 40 2-1-04-0
Type 2/3/4/5/6 Only

2019/11/08 V0.1 Vic
Not Support Bristol APU

+1V2_DIMM
GND

M_MA_B0	AC36	MB_ADD[0]
M_MA_B1	U36	MB_ADD[1]
M_MA_B2	U37	MB_ADD[2]
M_MA_B3	T38	MB_ADD[3]
M_MA_B4	T37	MB_ADD[4]
M_MA_B5	R38	MB_ADD[5]
M_MA_B6	R36	MB_ADD[6]
M_MA_B7	P39	MB_ADD[7]
M_MA_B8	R38	MB_ADD[8]
M_MA_B9	P36	MB_ADD[9]
M_MA_B10	AC39	MB_ADD[10]
M_MA_B11	P37	MB_ADD[11]
M_MA_B12	N38	MB_ADD[12]
M_MA_B13	AG38	MB_ADD[13]
M_ACT_B_N	M38	MB_ACT_L
M_BG_B0	M36	MB_BG[0]
M_BG_B1	M39	MB_BG[1]
M_BS_B0	AD38	MB_BANK[0]
M_BS_B1	AC37	MB_BANK[1]
M_DM_B0	C21	MB_DM[0]
M_DM_B1	D26	MB_DM[1]
M_DM_B2	A32	MB_DM[2]
M_DM_B3	D37	MB_DM[3]
M_DM_B4	AL38	MB_DM[4]
M_DM_B5	AR39	MB_DM[5]
M_DM_B6	AT35	MB_DM[6]
M_DM_B7	AW29	MB_DM[7]
M_DM_B8	F39	MB_DM[8]
M_DQS_B_P0	B22	MB_DQS_H[0]
M_DQS_B_N0	A22	MB_DQS_L[0]
M_DQS_B_P1	C27	MB_DQS_L[1]
M_DQS_B_N1	B27	MB_DQS_L[1]
M_DQS_B_P2	C33	MB_DQS_L[2]
M_DQS_B_N2	C32	MB_DQS_L[2]
M_DQS_B_P3	B37	MB_DQS_L[3]
M_DQS_B_N3	A37	MB_DQS_L[3]
M_DQS_B_P4	AM37	MB_DQS_L[4]
M_DQS_B_N4	AM36	MB_DQS_L[4]
M_DQS_B_P5	AT38	MB_DQS_L[5]
M_DQS_B_N5	AT39	MB_DQS_L[5]
M_DQS_B_P6	AU34	MB_DQS_L[6]
M_DQS_B_N6	AV34	MB_DQS_L[6]
M_DQS_B_P7	AU28	MB_DQS_L[7]
M_DQS_B_N7	AU29	MB_DQS_L[7]
M_DQS_B_P8	G38	MB_DQS_L[8]
M_DQS_B_N8	G37	MB_DQS_L[8]
M_CLK_B_P0	U39	MB_CLK_H[0]
M_CLK_B_N0	V39	MB_CLK_L[0]
M_CLK_B_P1	V38	MB_CLK_H[1]
M_CLK_B_N1	W38	MB_CLK_L[1]
M_CLK_B_P2	W37	MB_CLK_H[2]
M_CLK_B_N2	Y37	MB_CLK_L[2]
M_CLK_B_P3	Y39	MB_CLK_H[3]
M_CLK_B_N3	AA39	MB_CLK_L[3]
M_DRAMRST_B_L	K35	MB_RESET_L
M_EVENT_B_L	AA38	MB_EVENT_L
M_CKE_B0	L37	MBO_CKE[0]
M_CKE_B1	K37	MBO_CKE[1]
M_CKE_B2	L39	MBO_CKE[2]
M_CKE_B3	L36	MBO_CKE[3]
M_ODT_B0	AF39	MBO_ODT[0]
M_ODT_B1	AH36	MBO_ODT[1]
M_ODT_B2	AF37	MBO_ODT[2]
M_ODT_B3	AH38	MBO_ODT[3]
M_CS_B_L0	AE37	MBO_CS_L[0]
M_CS_B_L1	AG39	MBO_CS_L[1]
M_CS_B_L2	AE38	MBO_CS_L[2]
M_CS_B_L3	AG36	MBO_CS_L[3]
M_MA_B17	AH37	MB_ADD_17
M_MA_B16	AD36	MB_RAS_L_ADD[16]
M_MA_B15	AF36	MB_CAS_L_ADD[15]
M_MA_B14	AD39	MB_WE_L_ADD[14]
M_ALERT_B_L	N37	MB_ALERT_L
M_PARITY_B	AB38	MB_PAROUT

Type 0 Only
R620 1 2 39 2-1-04-0
R575 1 2 40 2-1-04-0
Type 2/3/4/5/6 Only

2019/11/08 V0.1 Vic
Not Support Bristol APU

+1V2_DIMM
GND

D20	M_DATA_B0
B21	M_DATA_B1
B24	M_DATA_B2
C24	M_DATA_B3
A20	M_DATA_B4
C30	M_DATA_B5
A30	M_DATA_B6
C23	M_DATA_B7
A26	M_DATA_B8
C26	M_DATA_B9
A29	M_DATA_B10
C29	M_DATA_B11
A25	M_DATA_B12
B25	M_DATA_B13
A28	M_DATA_B14
B28	M_DATA_B15
A31	M_DATA_B16
B31	M_DATA_B17
B34	M_DATA_B18
C35	M_DATA_B19
B30	M_DATA_B20
C30	M_DATA_B21
B33	M_DATA_B22
A34	M_DATA_B23
B36	M_DATA_B24
E36	M_DATA_B25
C39	M_DATA_B26
D38	M_DATA_B27
A35	M_DATA_B28
C36	M_DATA_B29
B38	M_DATA_B30
C38	M_DATA_B31
AK39	M_DATA_B32
AL37	M_DATA_B33
AN38	M_DATA_B34
AN39	M_DATA_B35
AK38	M_DATA_B36
AK36	M_DATA_B37
AM39	M_DATA_B38
AN38	M_DATA_B39
AR36	M_DATA_B40
AR37	M_DATA_B41
AU37	M_DATA_B42
AV37	M_DATA_B43
AP37	M_DATA_B44
AF38	M_DATA_B45
AT36	M_DATA_B46
AU38	M_DATA_B47
AW35	M_DATA_B48
AU35	M_DATA_B49
AW32	M_DATA_B50
AU32	M_DATA_B51
AV36	M_DATA_B52
AW36	M_DATA_B53
AW33	M_DATA_B54
AV33	M_DATA_B55
AW30	M_DATA_B56
AV30	M_DATA_B57
AW27	M_DATA_B58
AW26	M_DATA_B59
AU31	M_DATA_B60
AU31	M_DATA_B61
AV28	M_DATA_B62
AV27	M_DATA_B63
F38	M_DATA_B_CB0
F36	M_DATA_B_CB1
H39	M_DATA_B_CB2
J39	M_DATA_B_CB3
E37	M_DATA_B_CB4
E39	M_DATA_B_CB5
H36	M_DATA_B_CB6
H37	M_DATA_B_CB7

Features	Pinnacle Ridge (Family 17h,00h-0Fh)	Raven Ridge(Raven-2) (Family 17h,20h-2Fh)
on-chip Graphics	NA	4 Display Engines, 3 DDI Ports

Features	Raven Ridge(Raven-1)/ Picasso (Family 17h,10h-1Fh)	Matisse (Family 17h,70h-7Fh)
on-chip Graphics	3 Display Engines, 2 DDI Ports	NA

To HDMI2 Co-lay DP2

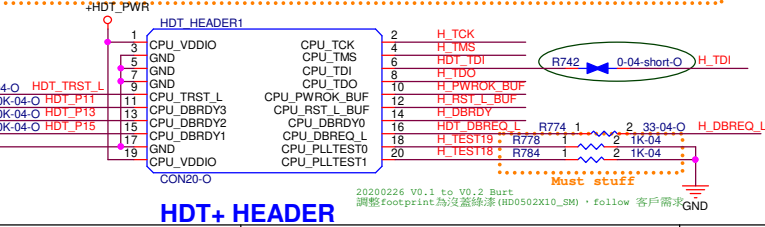
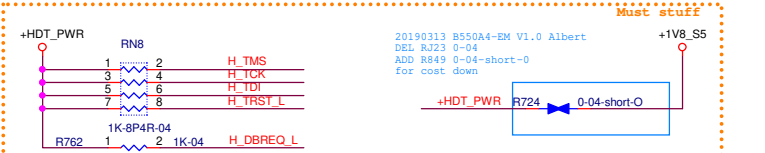
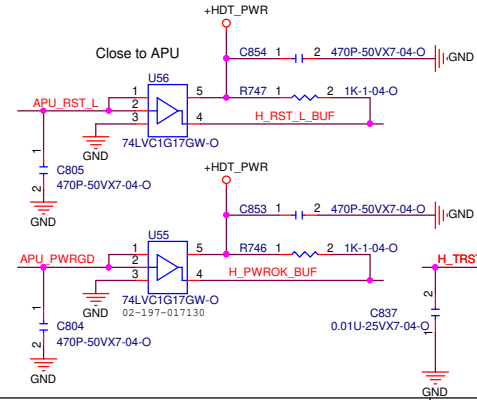
To DP Switch

20200213 V0.1 to V0.2 Burt
PWROK pull up to +1V8_S0 via 300 ohm
follow schematic check list

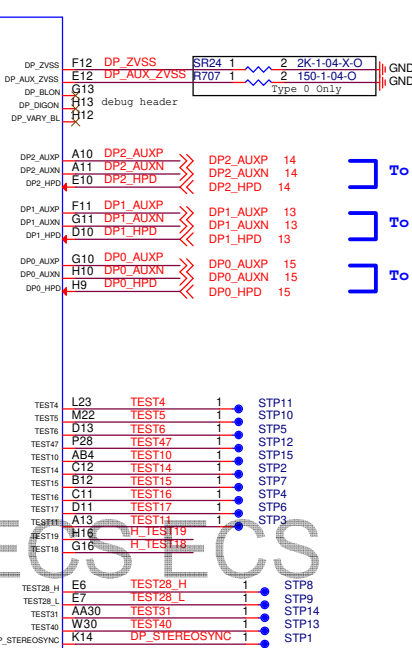
CORETYPE1	CORETYPE0	AM4 Processor Type	CRB
0	0	Type 0(Bristol Ridge)	BR
1	0	Type 2(Pinnacle Ridge)	ZP
		Type 2(Summit Ridge)	
		Type 4(Matisse)	
		Type 6(Vermeer)	
1	1	Type 1(Raven Ridge-2)	RV
		Type 3(Raven Ridge-1)	
		Type 3(Raven Ridge-1)	
		Type 5(Renoir)	

APU PWROK C821 1 2 27P-04-O
APU_RST_L C772 1 2 0.01uF-25VX7-04
APU_PWRGD C807 1 2 27P-04-O
APU_SVT C759 1 2 27P-04-O

20200204 V0.1 to V0.2 Vic
R725 change from 300-04 to 1K-04 , Stuff C772
0.01uF-04 for solved signal quality issue



20200226 V0.1 to V0.2 Burt
調整footprint為沒蓋綠漆(HD0502X10_SM) , follow 客戶需求

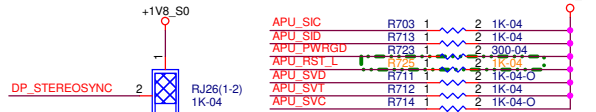


To HDMI2

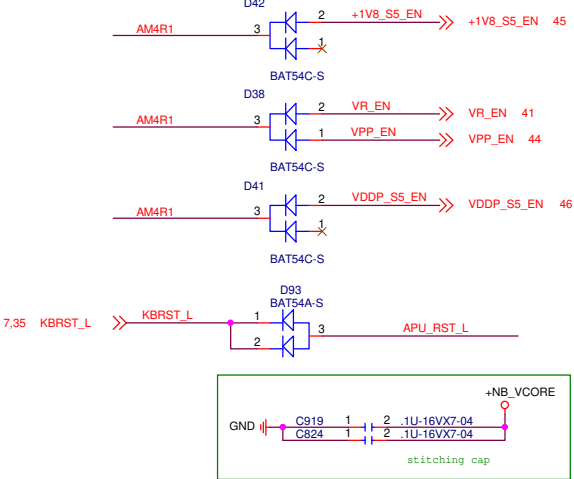
To HDMI1 Co-lay DP1

To DP Switch

20200204 V0.1 to V0.2 Vic
R725 change from 300-04 to 1K-04 , Stuff C772
0.01uF-04 for solved signal quality issue



RJ26	
1-2	HDMI enable.
2-3	HDMI disable.

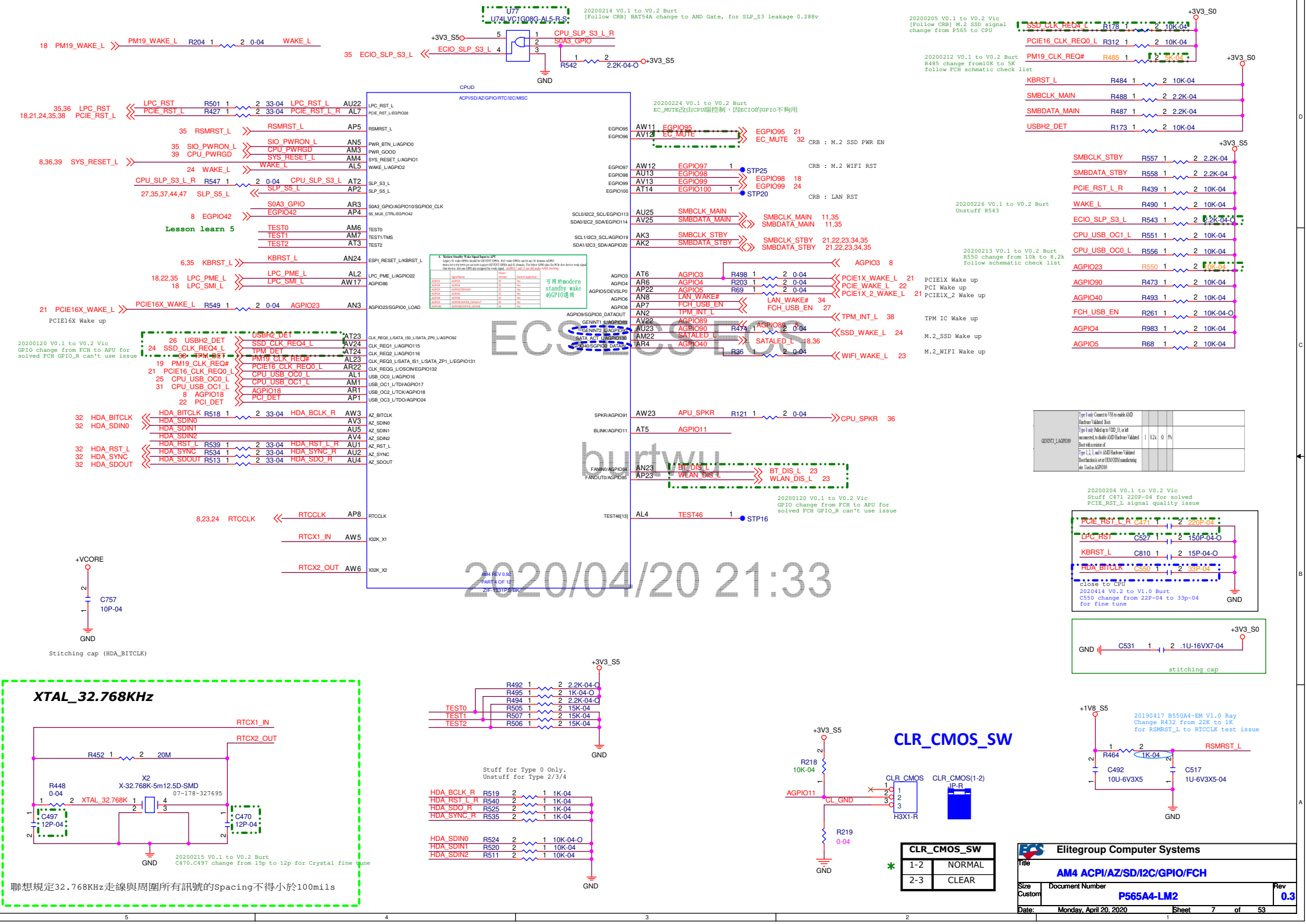


CORETYPE1	power rail	
0	+1V8_S0	Type 0(BR)
1	+3V3_S0	Type 2(SR/PR)
		Type 3(RR)
		Type 4(MTS)
		Type 5(Renoir)
1	+3V3_S0	Type 6(Vermeer)



41 VR_HOT_L VR_HOT_L R715 1 2 0-04 PROCHOT_L
35 APU_ALERT_L APU_ALERT_L R693 1 2 0-04 ALERT_L

Elitegroup Computer Systems			
Title	AM4 Display		
Size	Document Number	P565A4-LM2	Rev 0.3
Custom			
Date:	Monday, April 20, 2020	Sheet 6	of 53



20200214 V0.1 to V0.2 Burt
[Follow CRB] BAT54A change to AND Gate, for SLP_S3 leakage 0.28mv

20200205 V0.1 to V0.2 Vic
[Follow CRB] M.2 SSD signal
change from P565 to CPU

20200212 V0.1 to V0.2 Burt
R485 change from 10K to 5K
follow FCH schematic check list

20200224 V0.1 to V0.2 Burt
EC_MUTE改由CPU端控制，因ECIO的GPIO不夠用

20200226 V0.1 to V0.2 Burt
Unstuff R543

20200213 V0.1 to V0.2 Burt
R550 change from 10k to 8.2k
follow schematic check list

20200120 V0.1 to V0.2 Vic
GPIO change from FCH to APU for
solved FCH GPIO_R can't use issue

20200204 V0.1 to V0.2 Vic
Stuff C471 220P-04 for solved
PCIE_RST_L signal quality issue

20200120 V0.1 to V0.2 Vic
GPIO change from FCH to APU for
solved FCH GPIO_R can't use issue

20200414 V0.2 to V1.0 Burt
C550 change from 22P-04 to 33P-04
for fine tune

20200215 V0.1 to V0.2 Burt
C470,C497 change from 15p to 12p for Crystal fine tune

20190417 B550A4-EM V1.0 Ray
Change R432 from 22K to 1K
for RSMRST_L to RTCCLK test issue

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change from P565 to CPU

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Unstuff R543

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R550 change from 10k to 8.2k
follow schematic check list

20200120 V0.1 to V0.2 Vic
GPIO change from FCH to APU for
solved FCH GPIO_R can't use issue

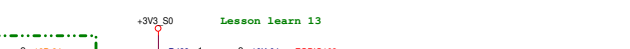
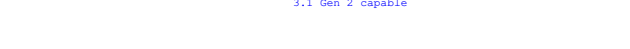
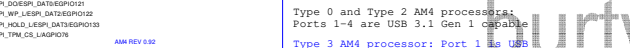
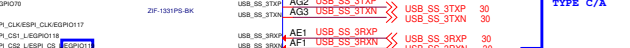
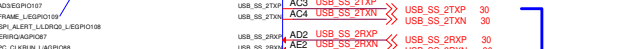
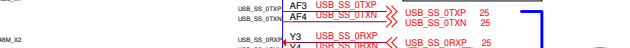
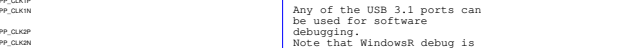
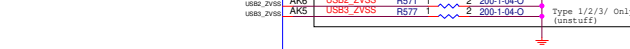
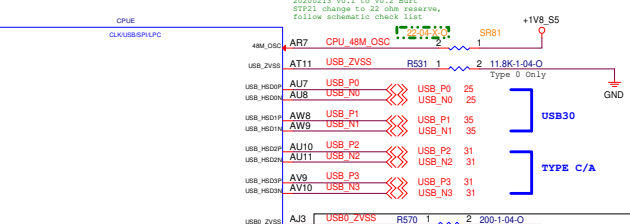
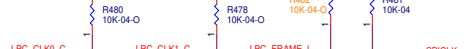
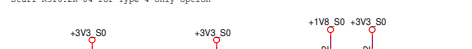
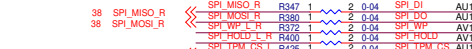
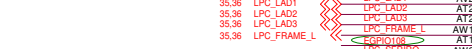
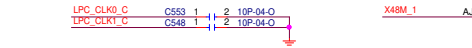
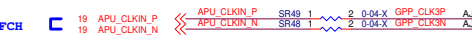
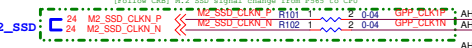
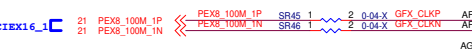
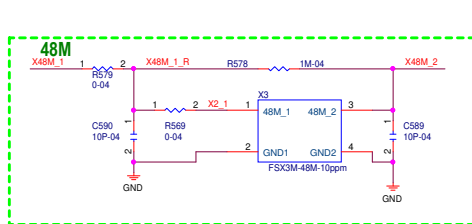
20200204 V0.1 to V0.2 Vic
Stuff C471 220P-04 for solved
PCIE_RST_L signal quality issue

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GPIO change from FCH to APU for
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C550 change from 22P-04 to 33P-04
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C470,C497 change from 15p to 12p for Crystal fine tune

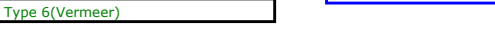
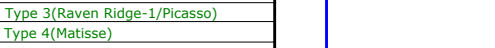
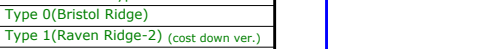
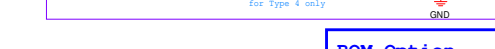
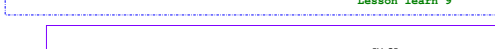
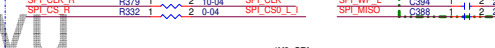
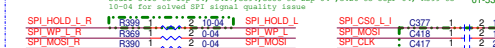
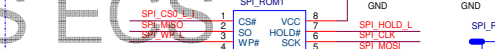
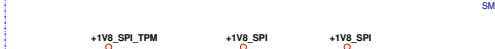
20190417 B550A4-EM V1.0 Ray
Change R432 from 22K to 1K
for RSMRST_L to RTCCLK test issue



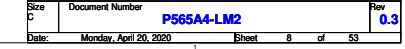
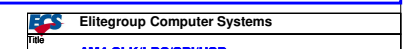
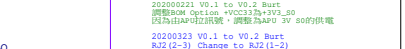
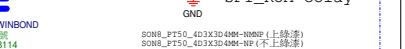
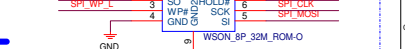
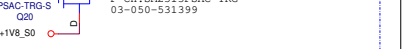
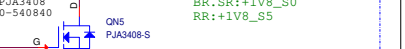
Type 0 AM4 processor: The 48M_OSC clock is active in S0 state only. Connect to devices that need a 48 MHz clock in S0 state only. This output is only enabled in S0 state. Voltage rail is VDD_33.

Type 2 and Type 3 AM4 processors: The 48M_OSC clock is active in S5 state. Connect to devices that need a 48 MHz clock in S5 state. When connecting to an S0 device the clock should be turned off by software when in the S5 state to prevent leakage. Voltage rail is VDD_18_S5.

USB 2.0 ports are not supported for Windows debug.



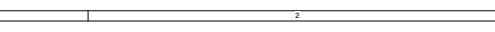
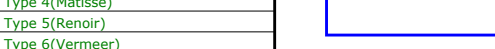
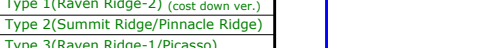
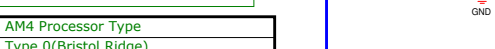
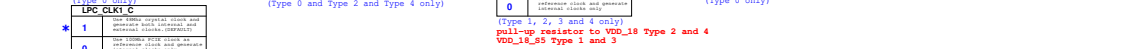
CORETYPE1	CORETYPE0	AM4 Processor Type
1	1	Type 1(RR)
1	0	Type 2(PR/SR)
1	1	Type3(Picasso)
1	0	Type4(Matisse)
1	1	Type5(Renoir)
1	0	Type6(Vermeer)



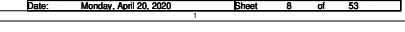
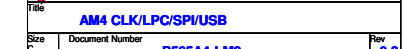
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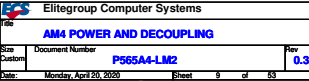
STRAP PINS

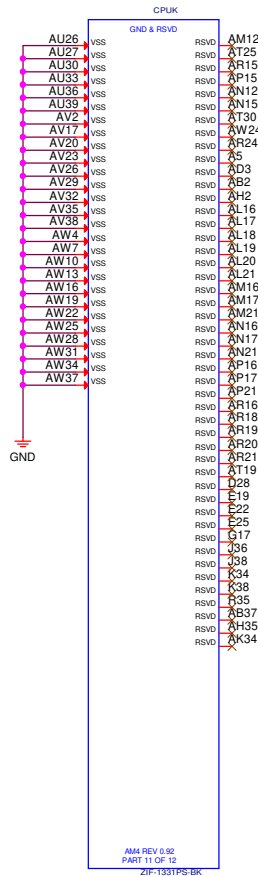
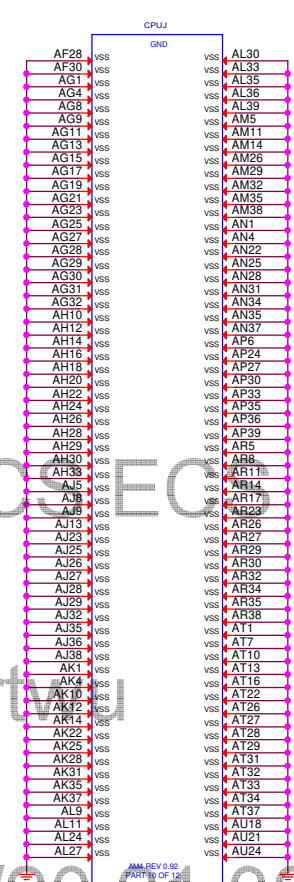
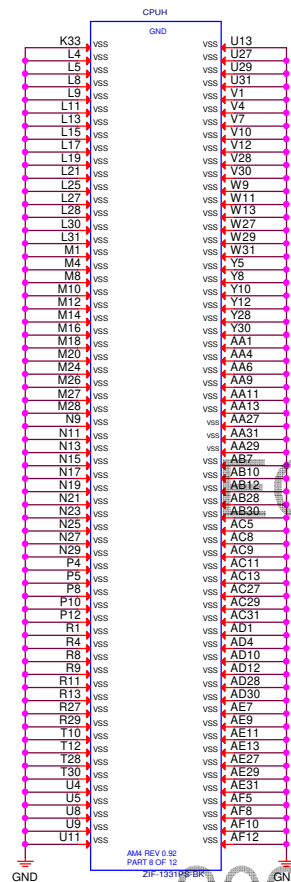
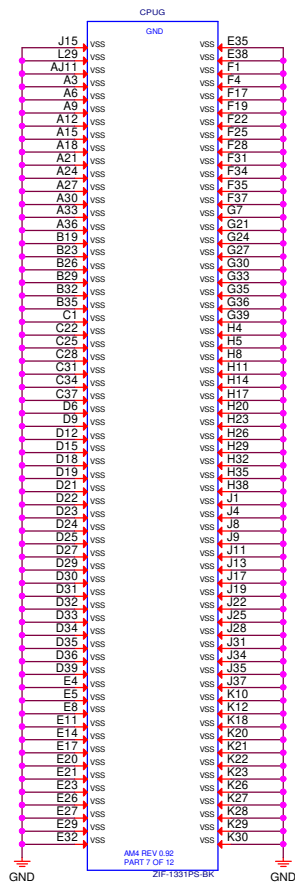
20190729 V1.0 to V1.0. Albert
Stuff R516:2K-04 for Type 4 only option



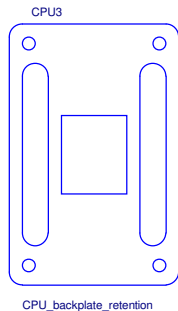
BOM Option





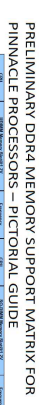


AMD AM4 socket P/N:
11-106-133121 SOCKET.CPU ZIF AM4..uPGA 1331P SMD..G/F...WHITE.AZIF0068-P002C...HF.LEAD-FREE.LOTES




H10 HOLE-A

H11 HOLE-A



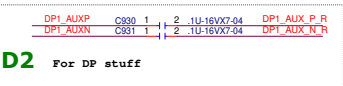
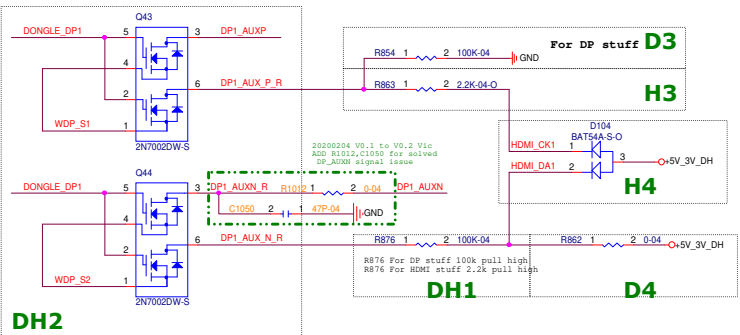
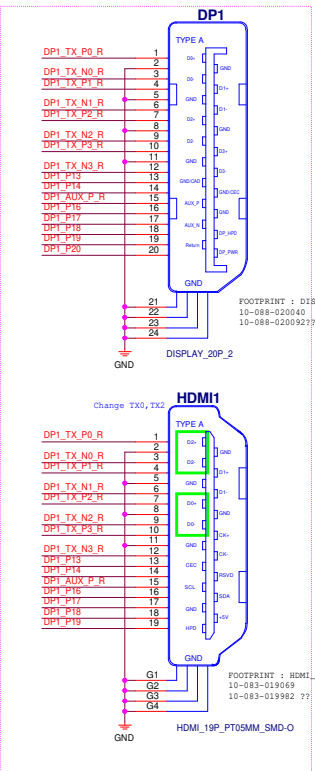
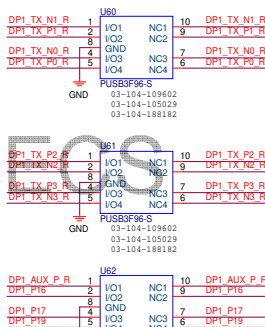
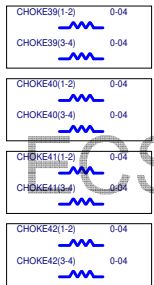
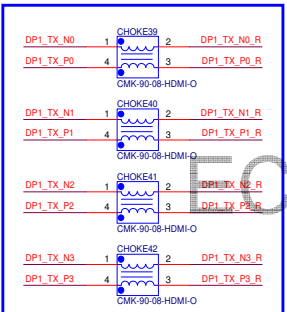
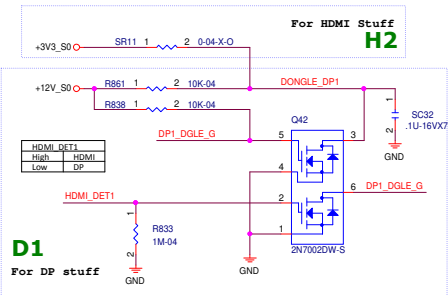
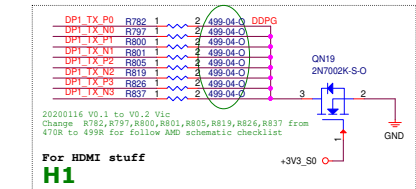
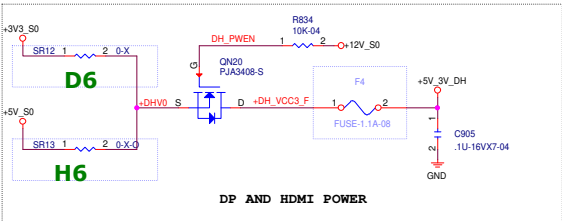
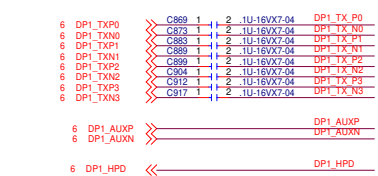
Memory Type	Board Layers	Number of DIMM Sockets	Number of DIMMs Populated	DIMM QDIMM	
				SR/DR	DIMM
UDIMM	4 or 6	1	1	SR/DR	N/A
		2	1	-	SR/DR
			2	SR/DR	SR/DR

[illegible]

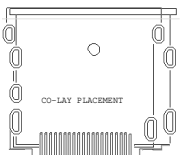
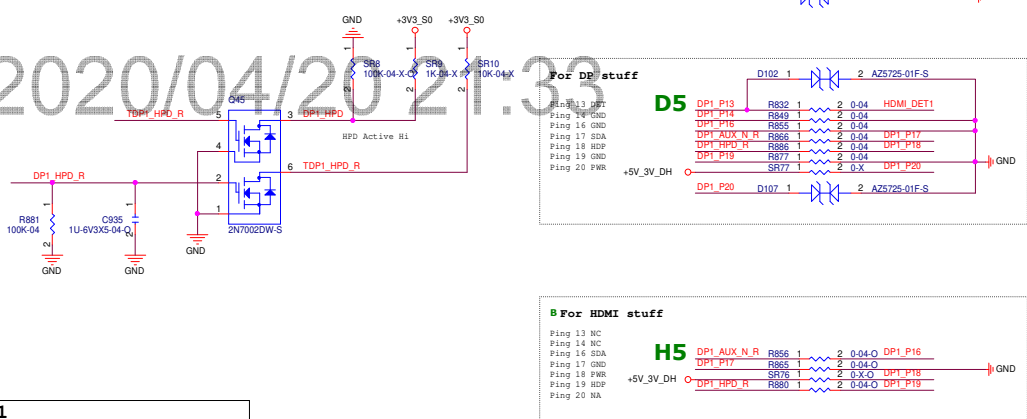


若使用 ICD20PM, 請注意 PA pin 18 or 17.

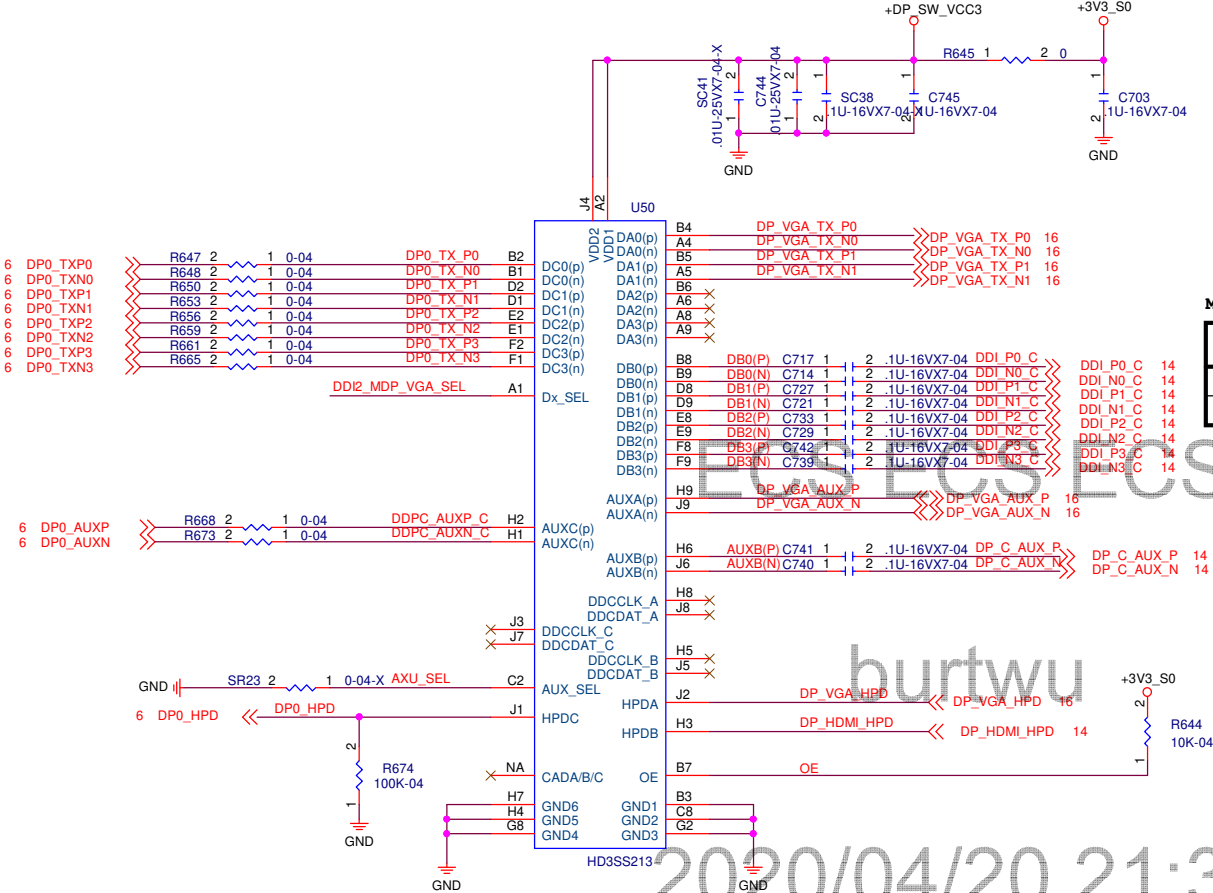
DP colay HDMI : Default DP



DP1 Co-lay HDMI1													
Location	D1	D2	D3	D4	D5	D6	H1	H2	H3	H4	H5	H6	H7
DP1	V	V	V	V	V	V	X	X	X	X	X	X	X
HDMI1	X	X	X	X	X	X	V	V	V	V	V	V	V



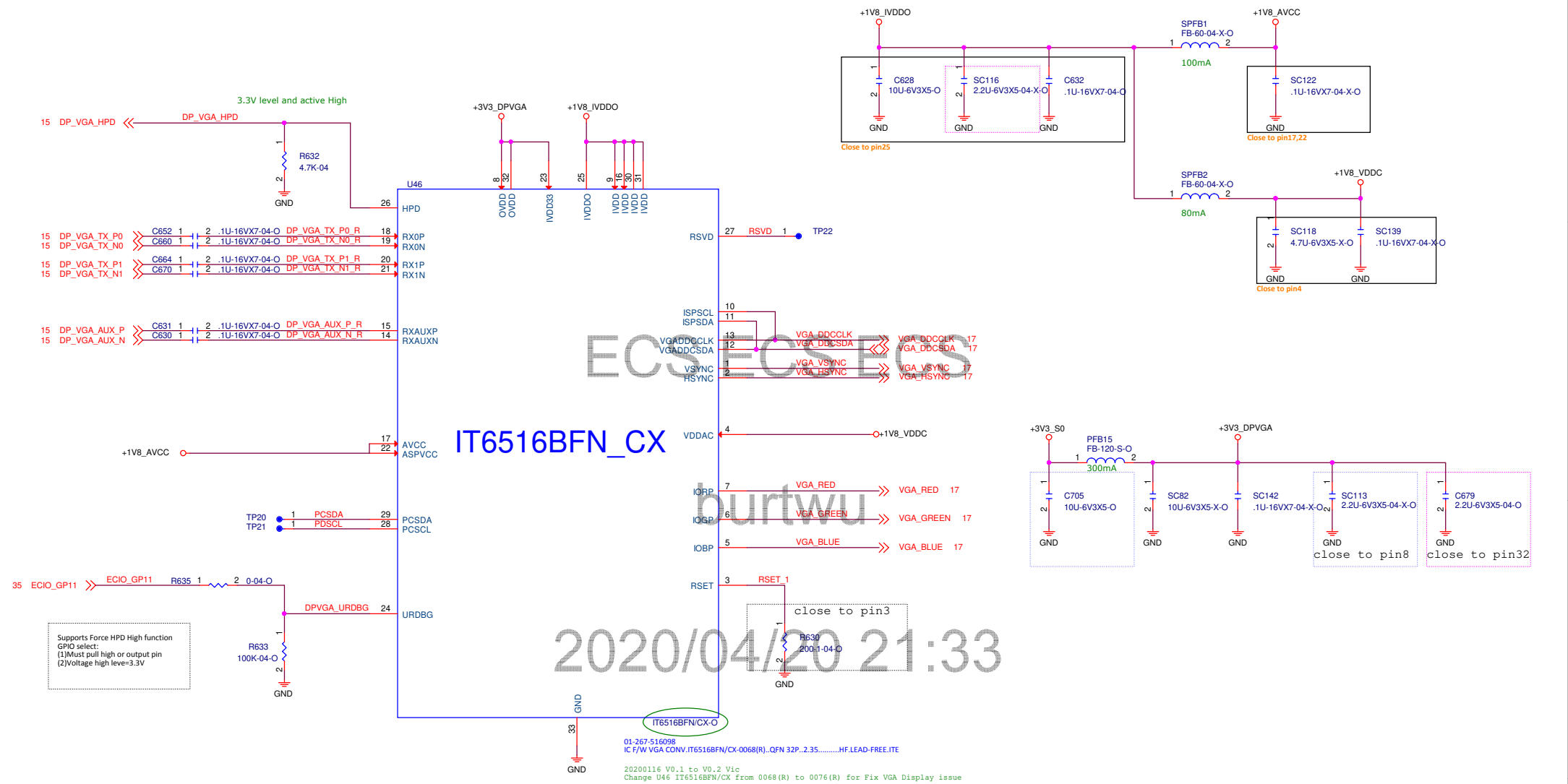
DP Differential Switch (HD3SS213)



MDP/VGA SELECT

Dx_SEL (A1)	AUX_SEL (C2)	DP/VGA	AUX/DDC
0V (L)	0V (L)	VGA	AUX
★ 3.3V (H)	0V (L)	DP	AUX

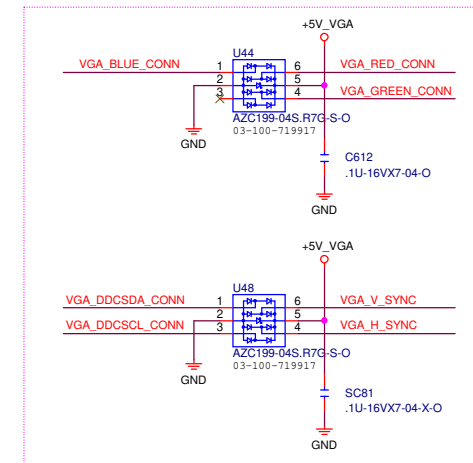
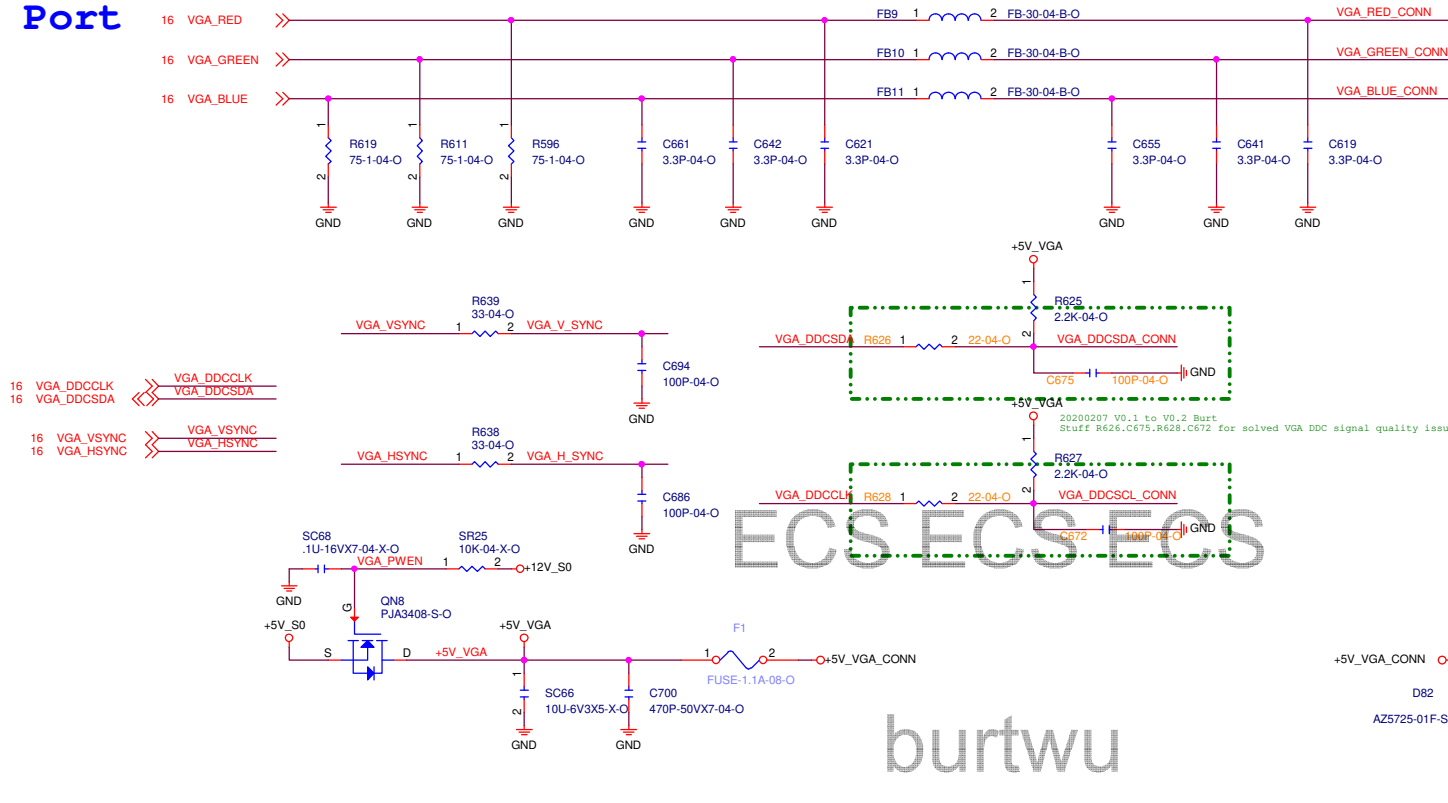
VGA BRIDGE (IT6516BFN-CX)



System Status	ECIO_GP11	It6516B'S HPD
Pre-OS (VBIOS/GOP)	High	Force High
Enter OS	Low	Depend on VGA device's plug/un-plug

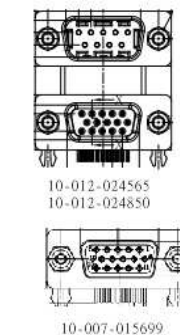
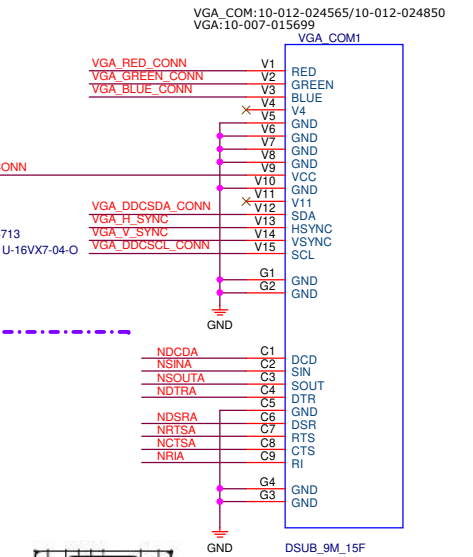
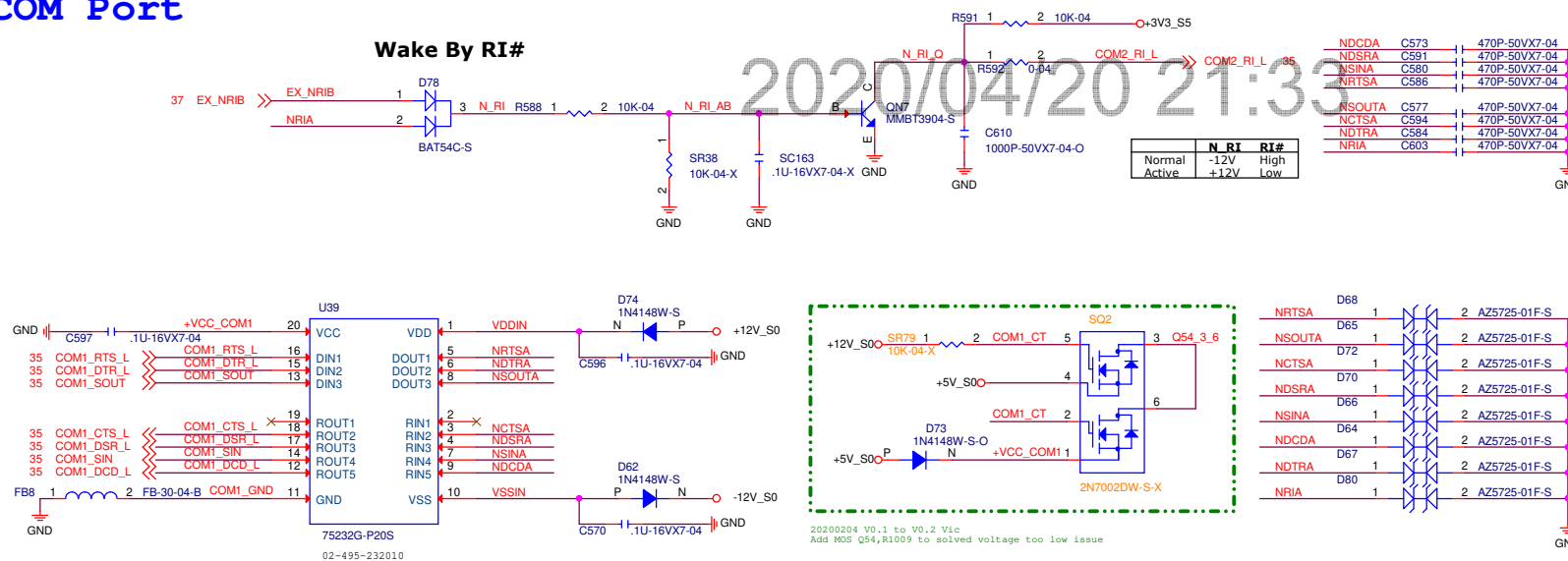
Version	Package	FW	HW
IT6516BFN-CX PN:01-267-516098	4 X 4mm 32pin QFN	V2.35	Support GPIO Control HPD Pin24:URDBG

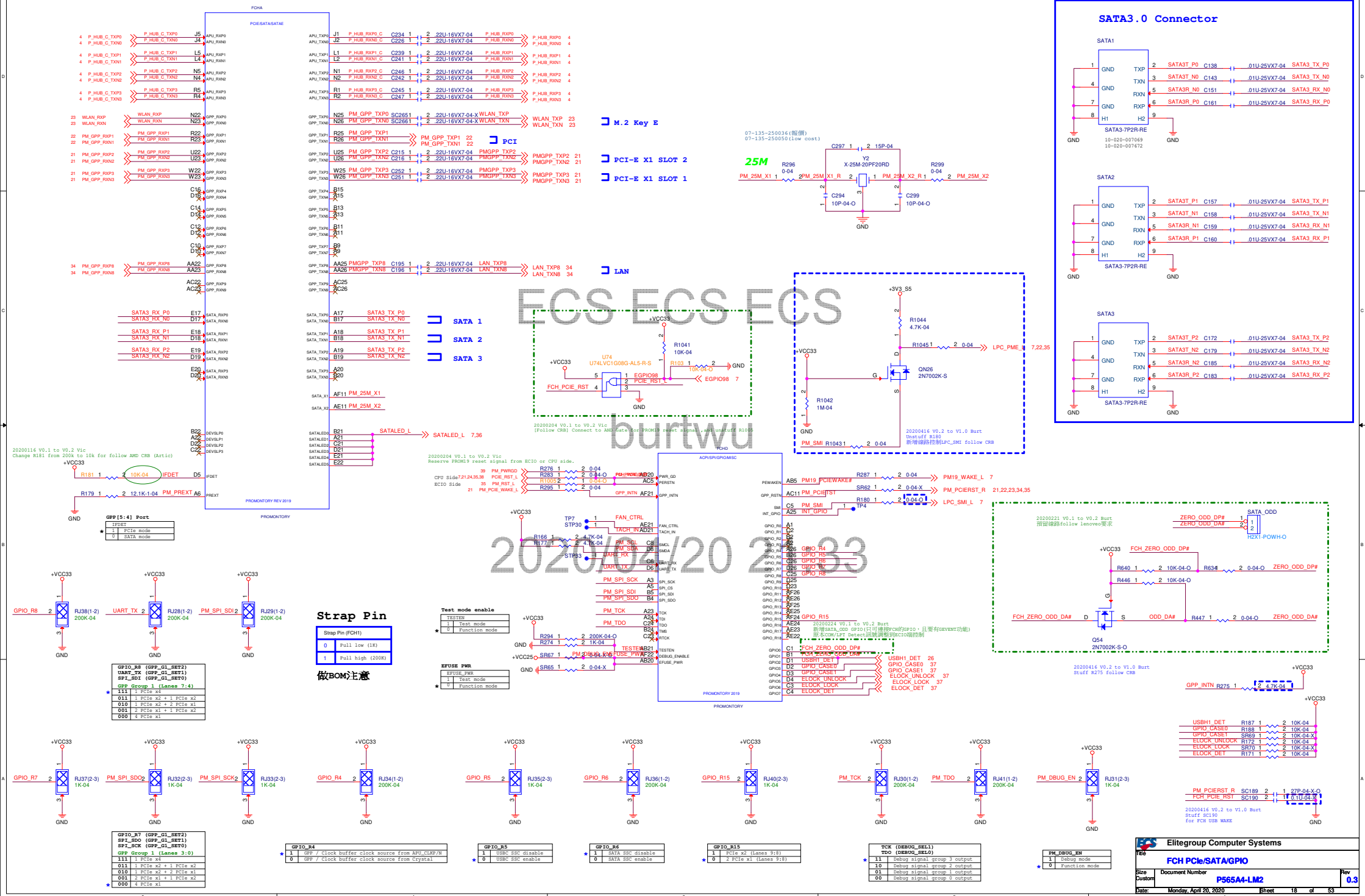
VGA Port

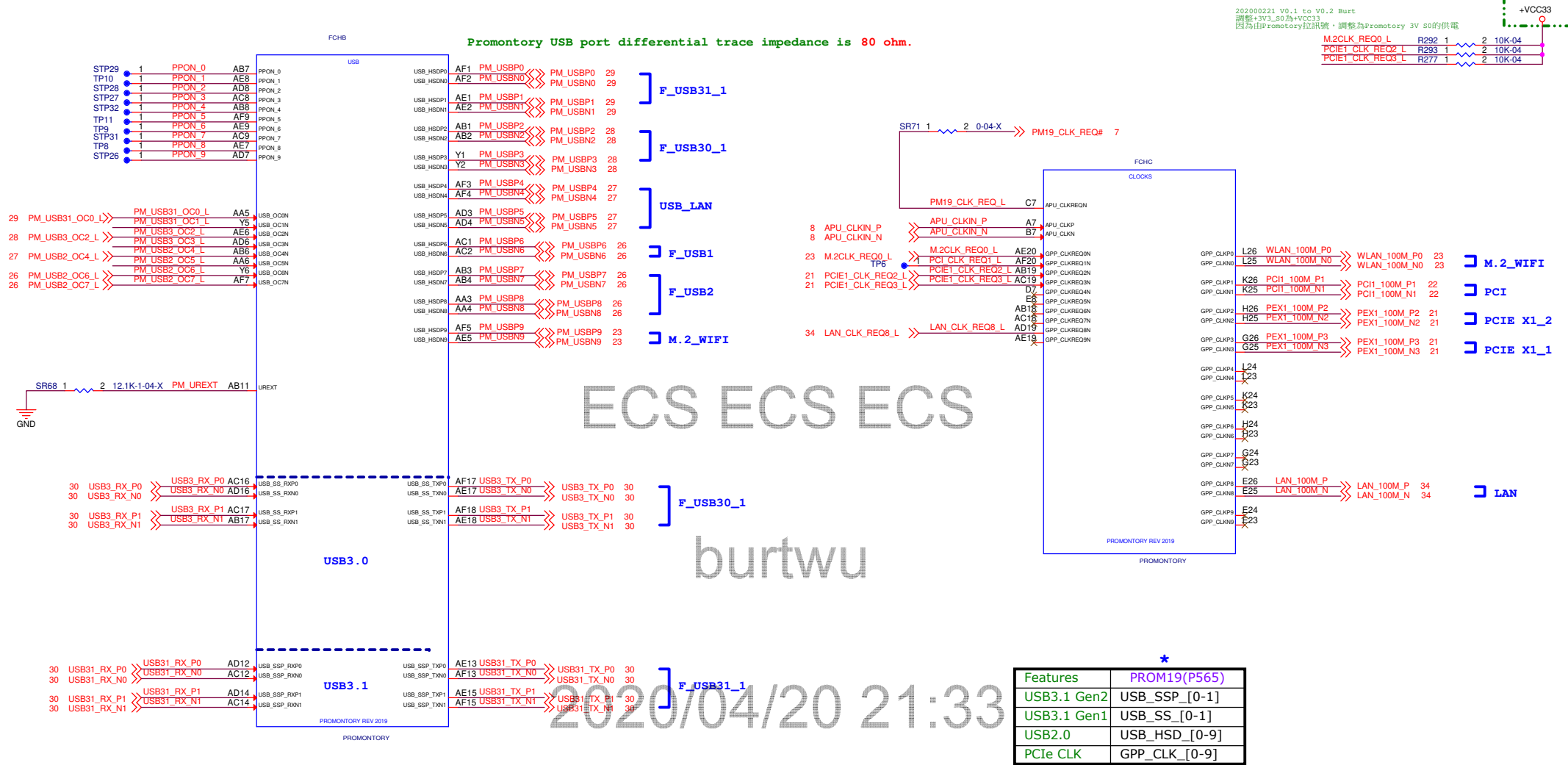


COM Port

Wake By RI#





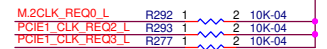


USB3.1 & USB2.0 & OC pin對應表

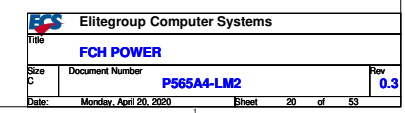
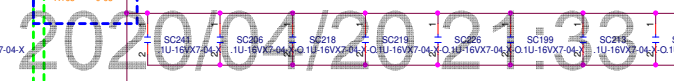
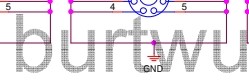
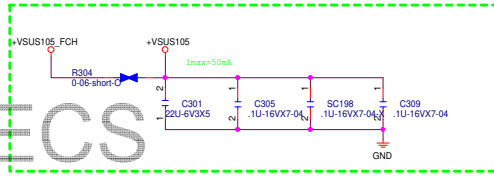
Table 13. USB Port to OC Pin Mapping		
USB 3.2 G2 (10 Gbps)	USB2.0	USB_OC
USB_SSP_TX/RX[0]	USB_HSDP/N[0]	USB_OC0N
USB_SSP_TX/RX[1]	USB_HSDP/N[1]	USB_OC1N
USB 3.2 G1 (5 Gbps)	USB2.0	USB_OC
USB_SS_TX/RX[0]	USB_HSDP/N[2]	USB_OC2N
USB_SS_TX/RX[1]	USB_HSDP/N[3]	USB_OC3N
	USB_HSDP/N[4]	USB_OC4N
	USB_HSDP/N[5]	USB_OC5N
	USB_HSDP/N[6]	USB_OC6N
	USB_HSDP/N[7]	USB_OC7N
	USB_HSDP/N[8]	USB_OC7N
	USB_HSDP/N[9]	USB_OC7N

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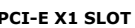
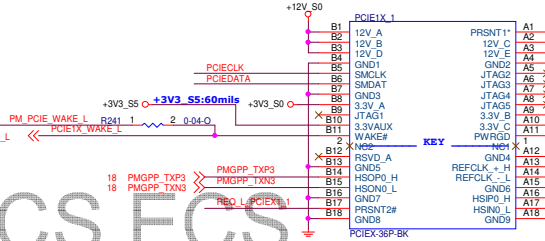
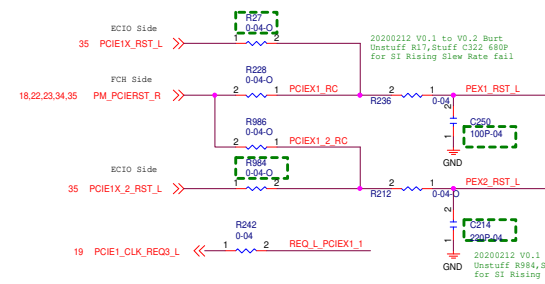
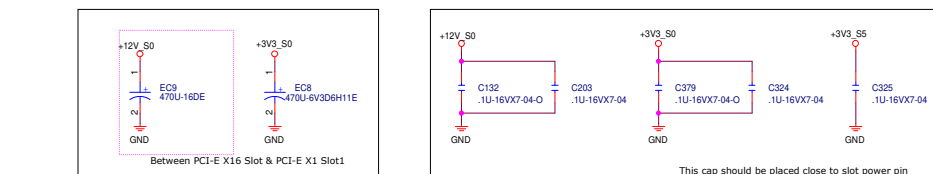
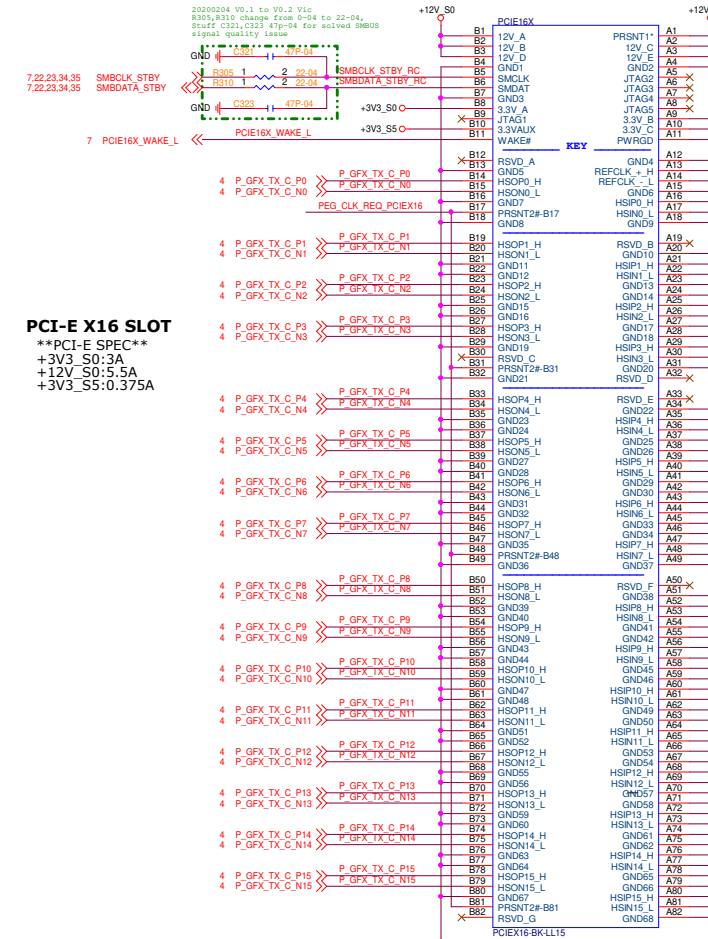
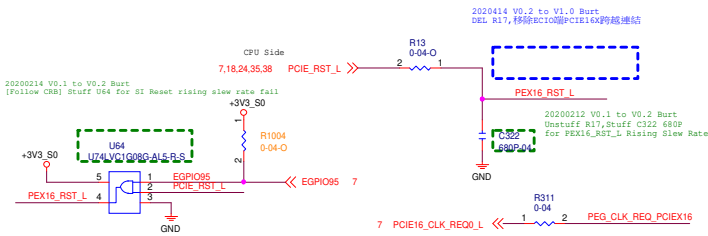
202000221 V0.1 to V0.2 Burt
調整+3V3_S0為+VCC33
因為由Promotory拉訊號，調整為Promotory 3V S0的供電



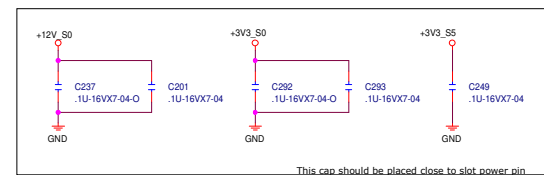
★	
Features	PROM19(P565)
USB3.1 Gen2	USB_SSP_[0-1]
USB3.1 Gen1	USB_SS_[0-1]
USB2.0	USB_HSD_[0-9]
PCIe CLK	GPP_CLK_[0-9]



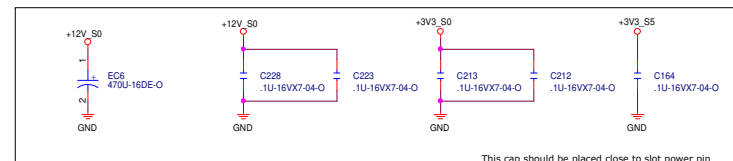
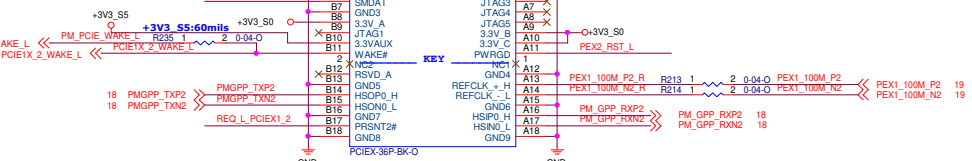
PCIE X16 / X1 Slot



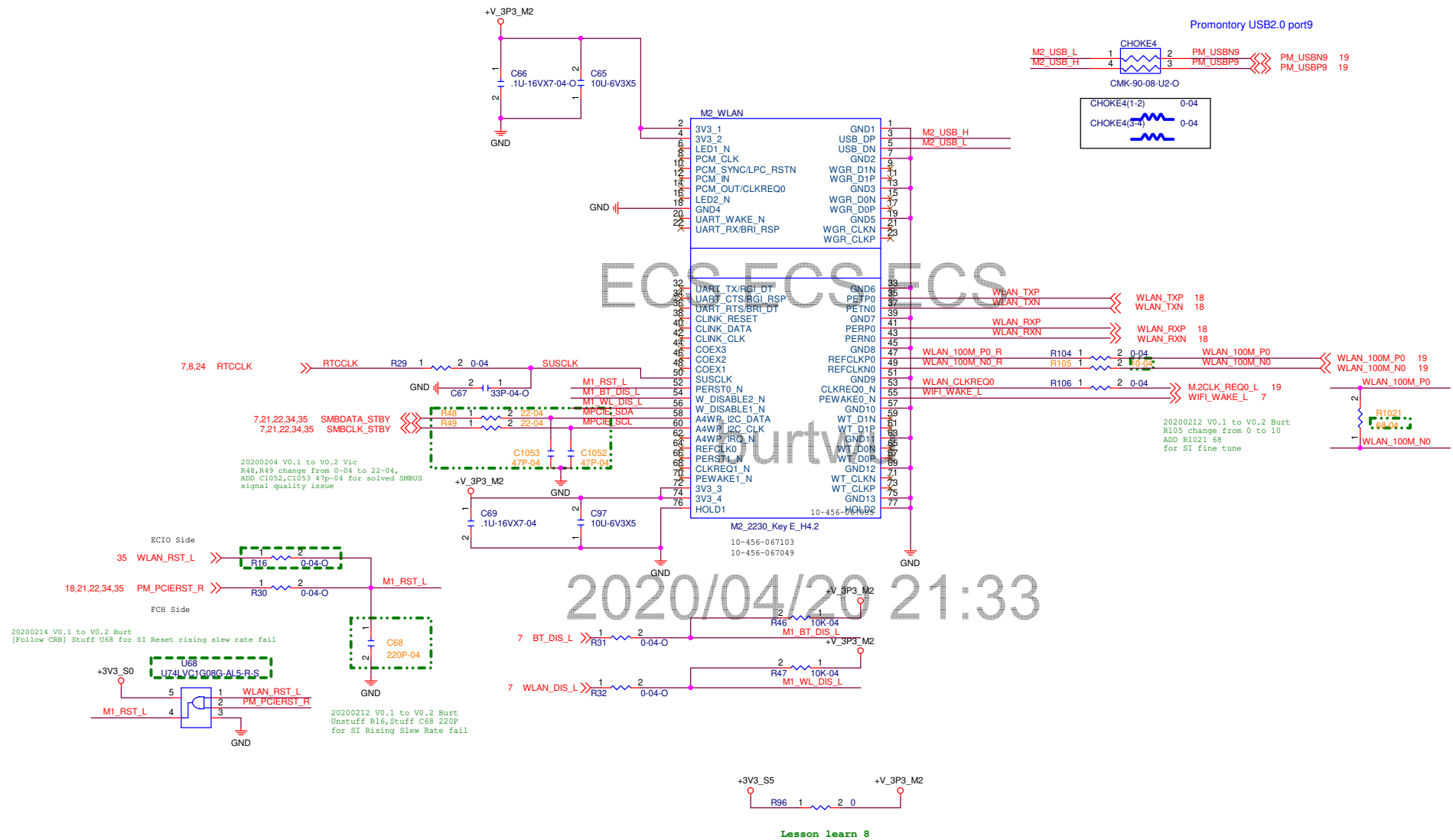
```
**PCI-E SPEC**
+3V3_S0:3A
+12V_S0:0.5A
+3V3_S5:0.375A
```



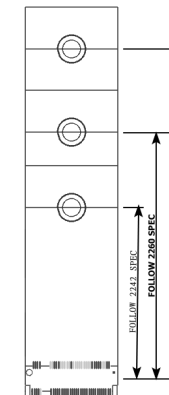
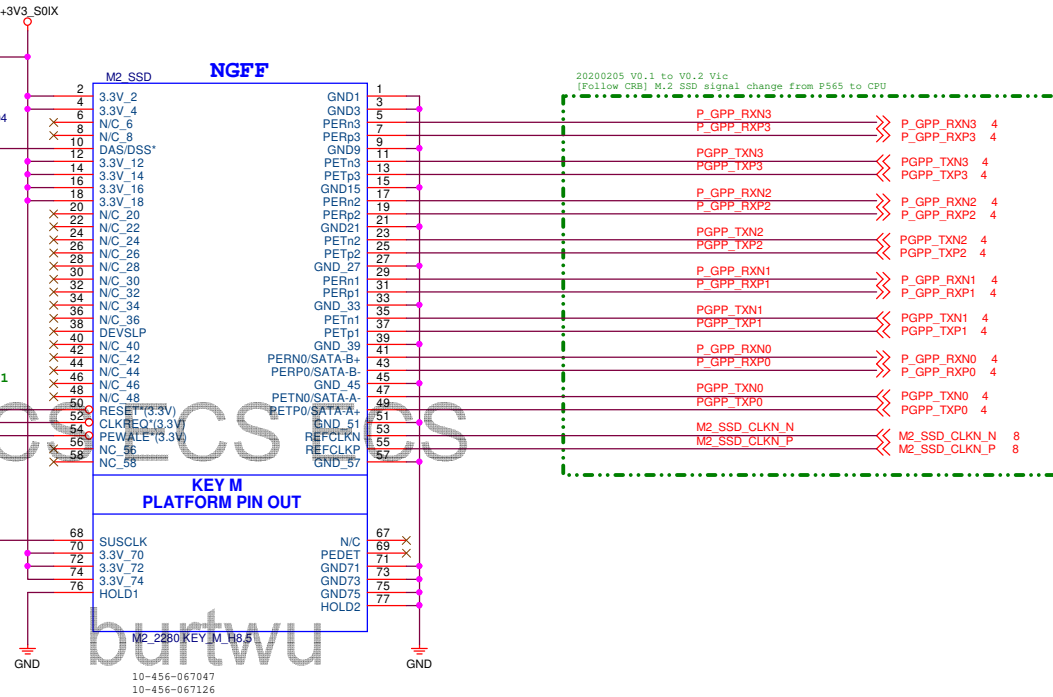
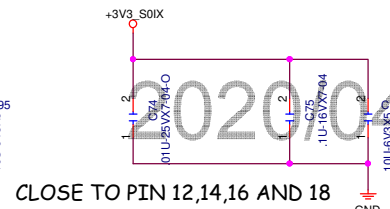
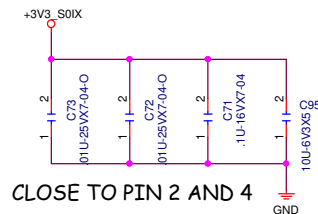
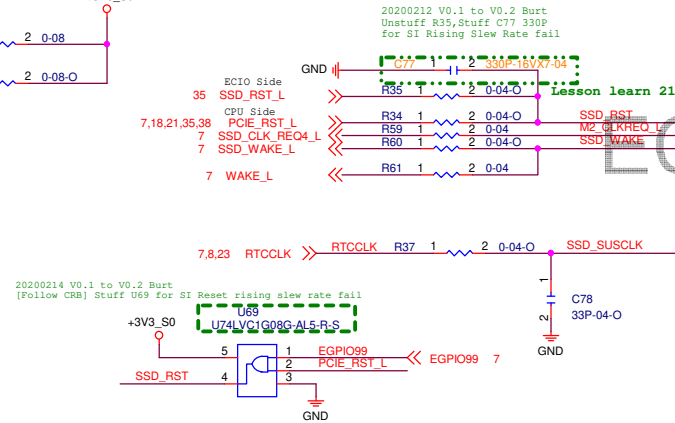
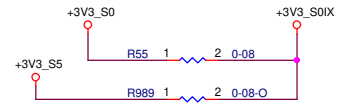
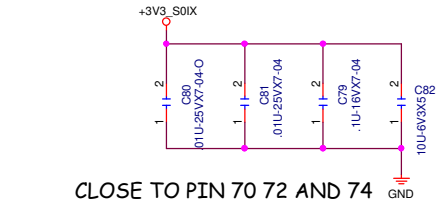
```
**PCI-E SPEC**
+3V3_S0:3A
+12V_S0:0.5A
+3V3_S5:0.375
```



M.2 Wifi & BT

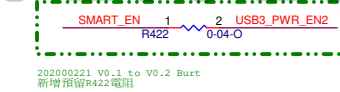
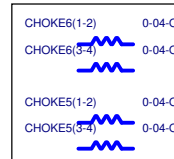
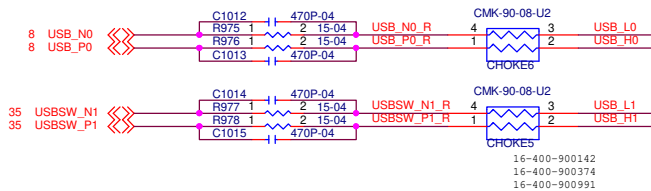
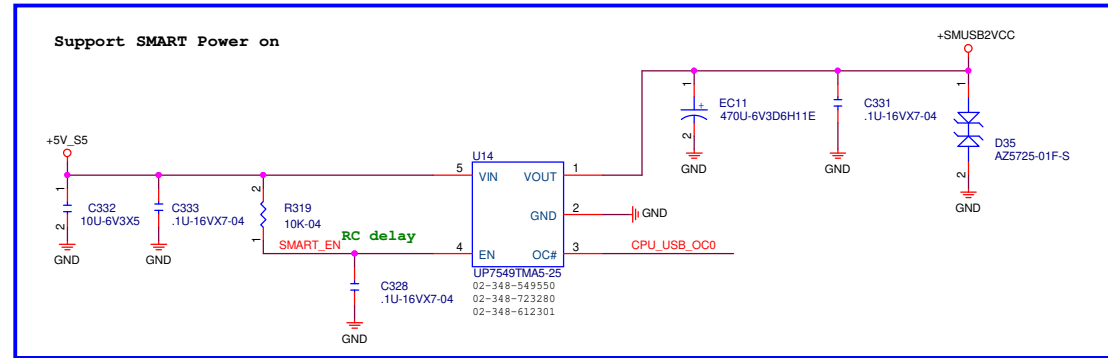


M.2 SSD (PCIe x4)



REAR USB3.1 GEN1 Connector

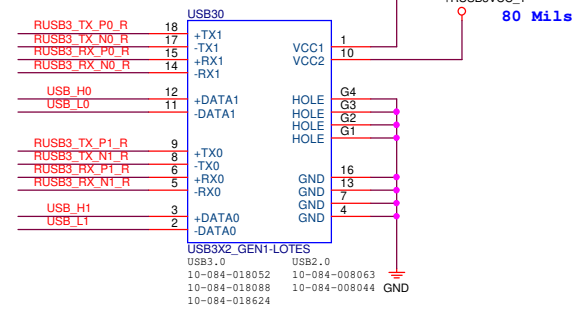
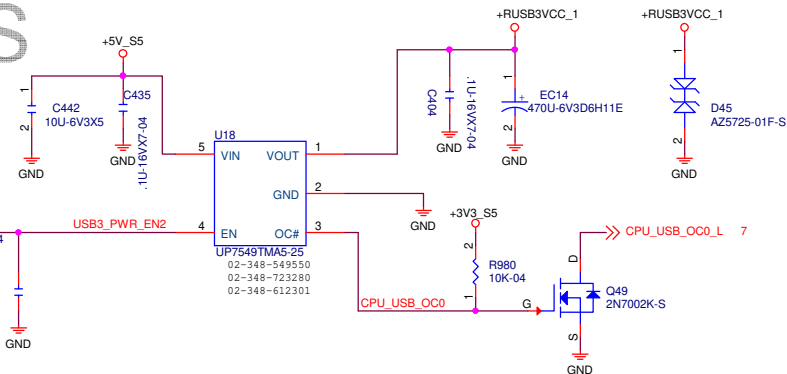
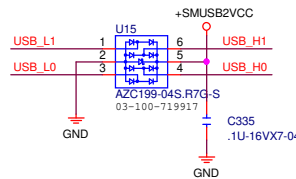
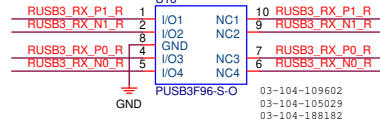
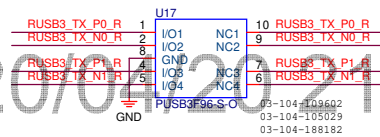
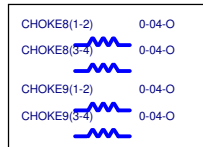
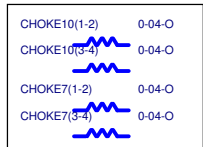
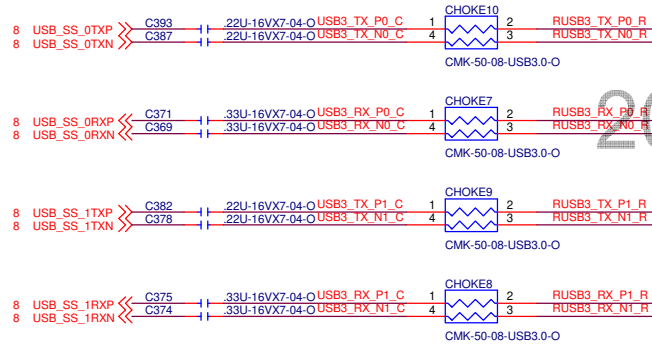
CPU USB3.0 port_0 / USB 2.0 port_0
CPU USB3.0 port_1 / USB 2.0 port_1



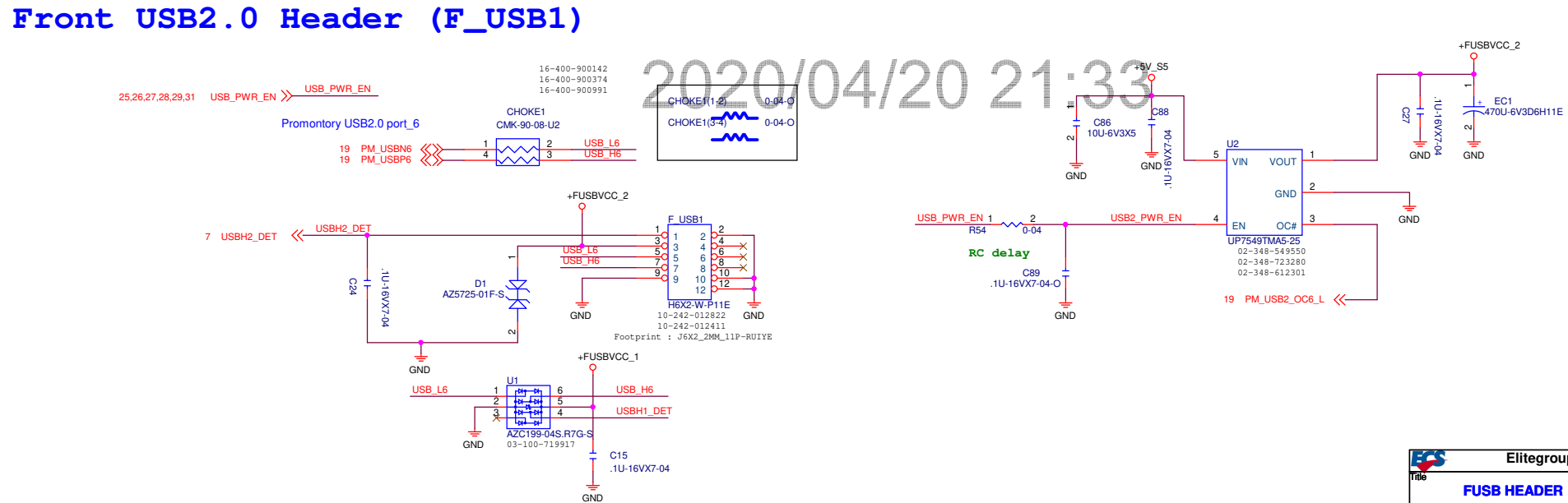
202000221 V0.1 to V0.2 Burt
新增預留R422電阻

26,27,28,29,31

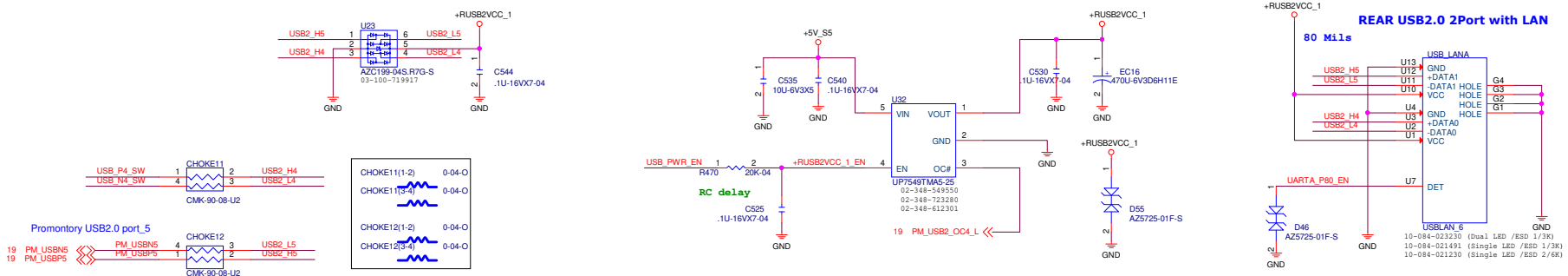
RC delay
C423
.1U-16VX7-04



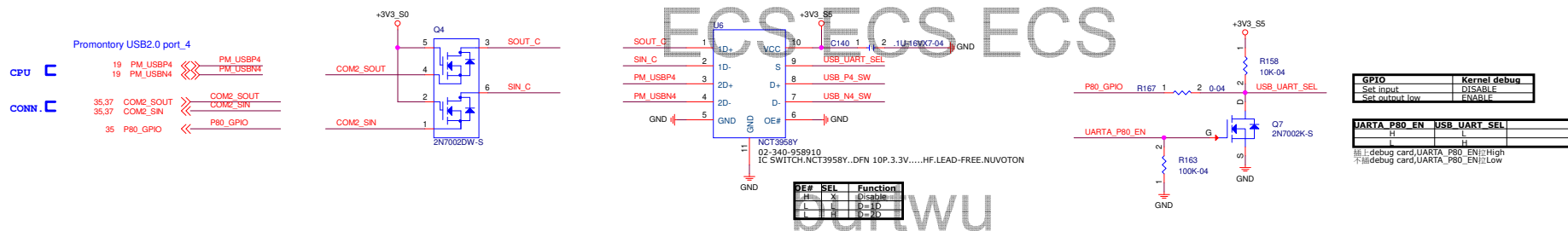
Front USB2.0 Header (F_USB1)



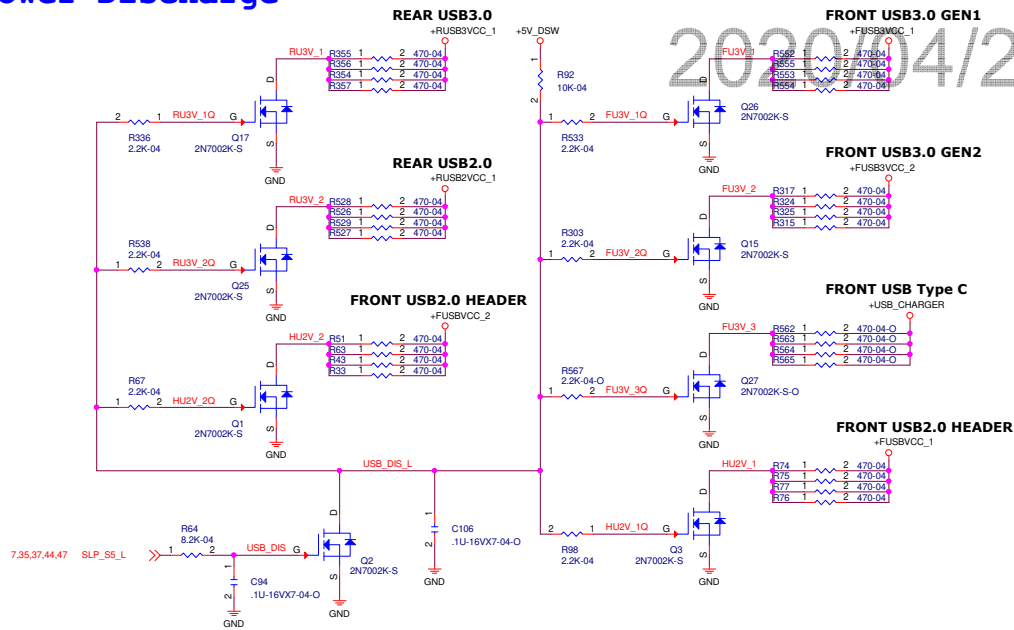
Rear USB2.0 Connector with LAN



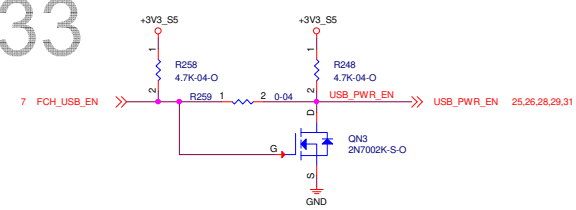
USB2.0 Switch



USB Power Discharge

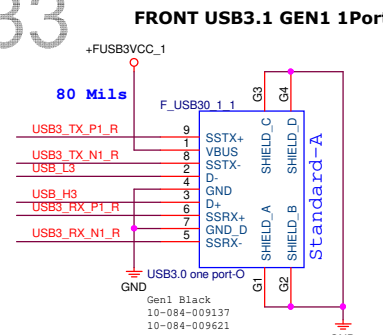
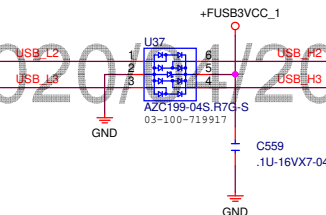
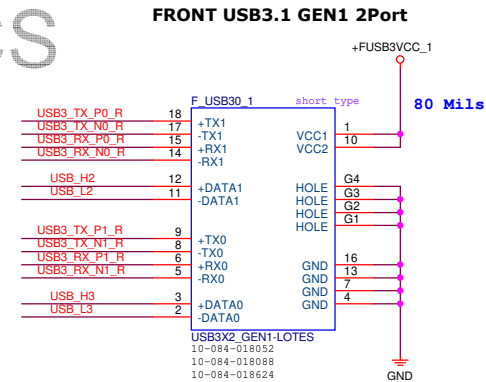
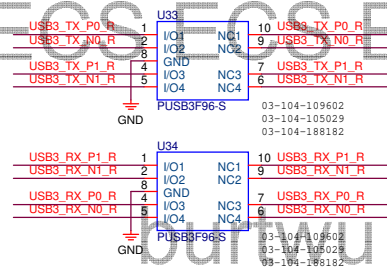
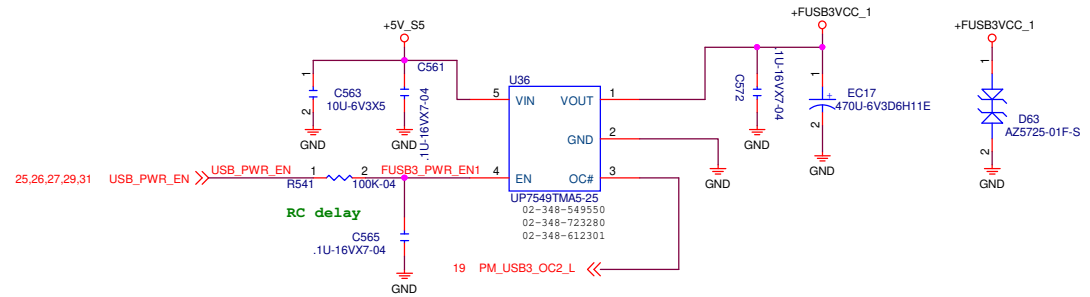
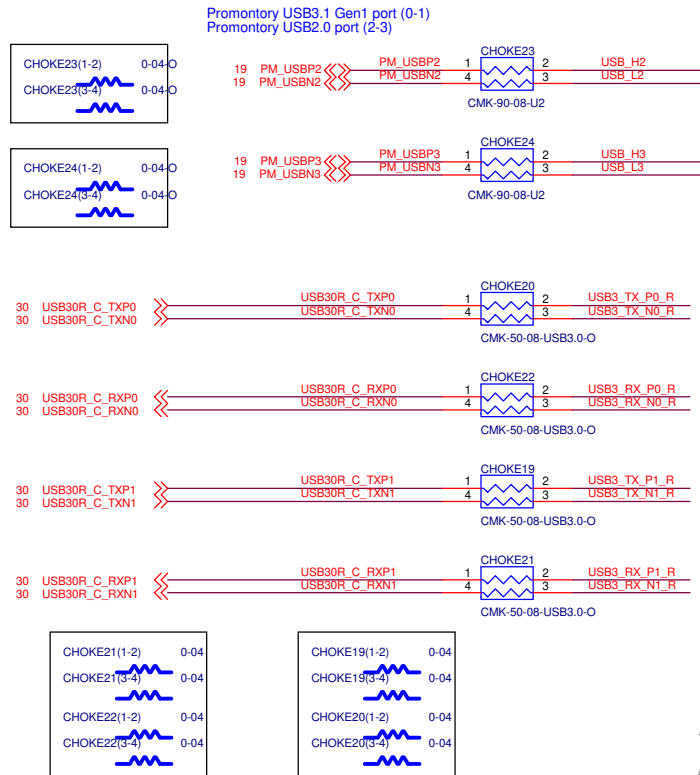


USB Power Enable



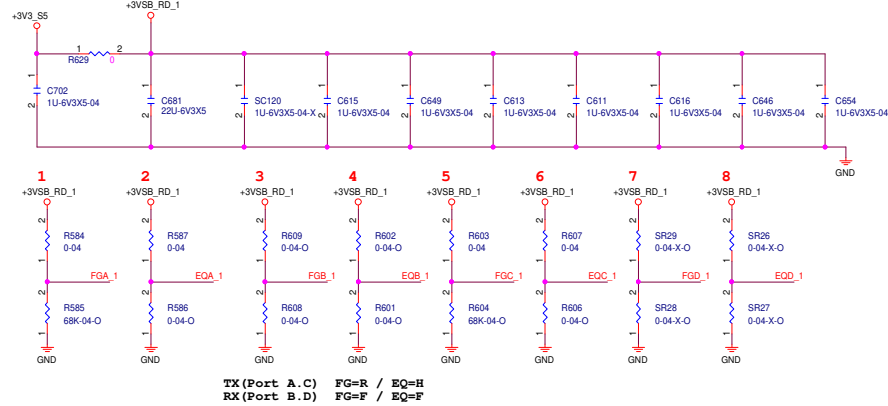
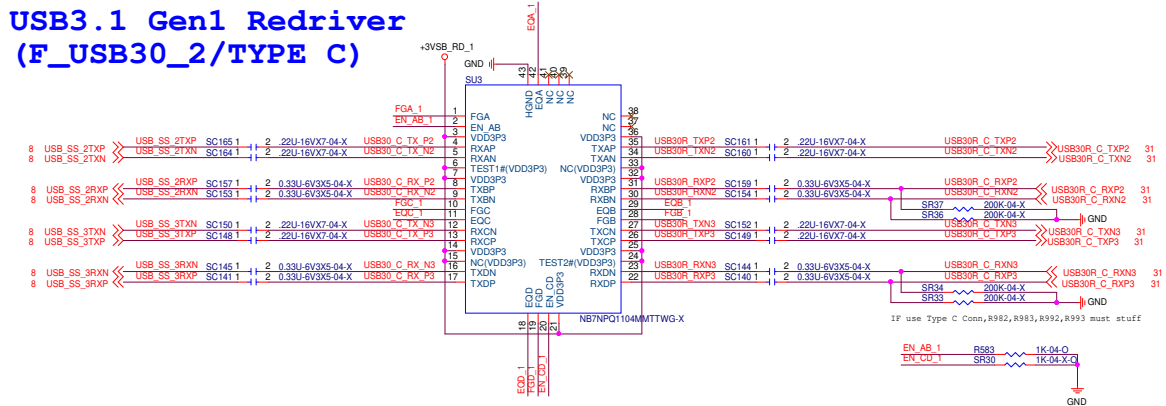
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Front USB3.1 Gen1 Connector

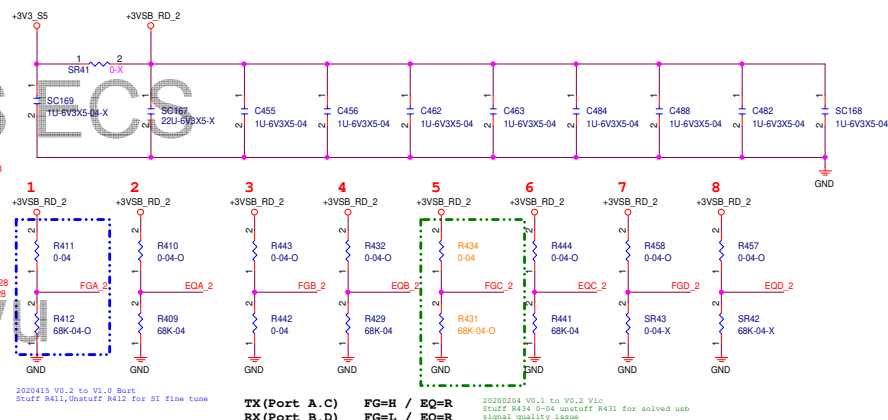
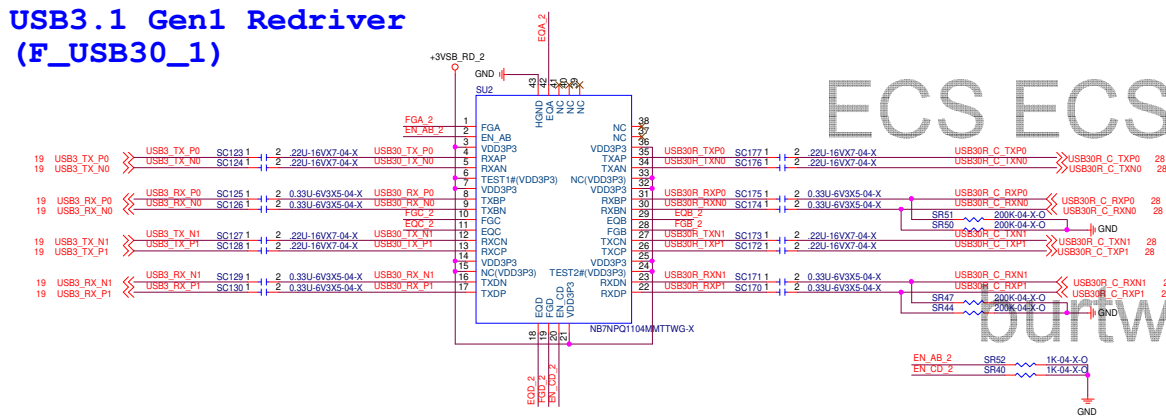


Dual port colay single port
Short type footprint

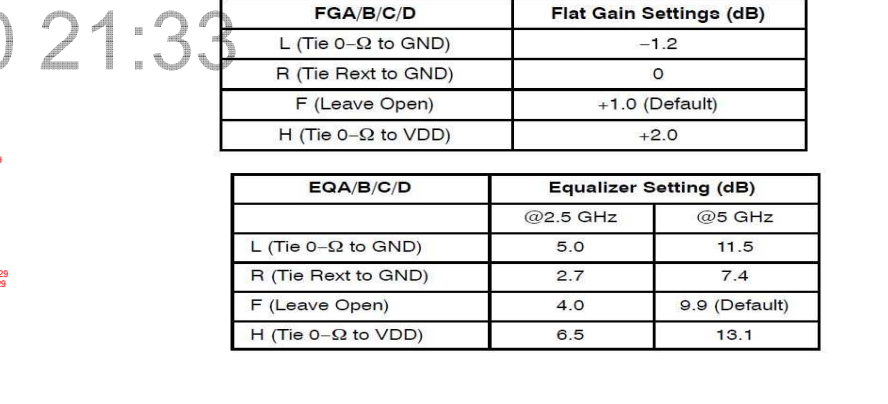
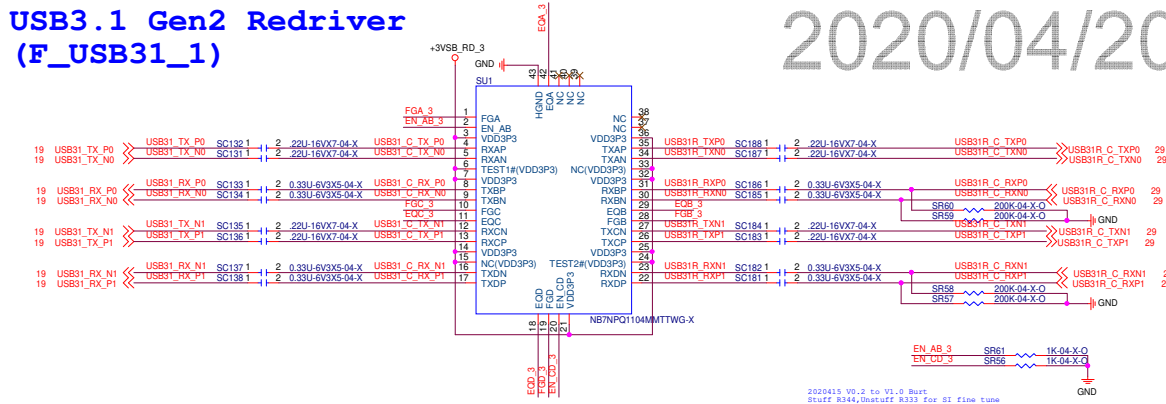
USB3.1 Gen1 Redriver (F_USB30_2/TYPE C)



USB3.1 Gen1 Redriver (F_USB30_1)

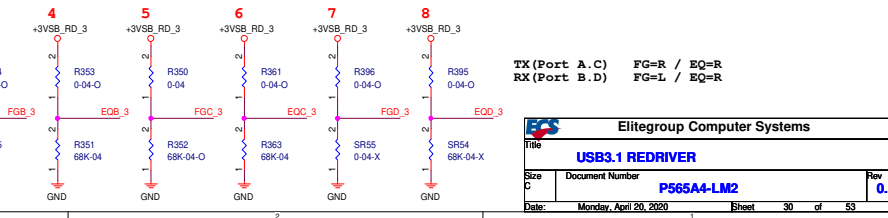
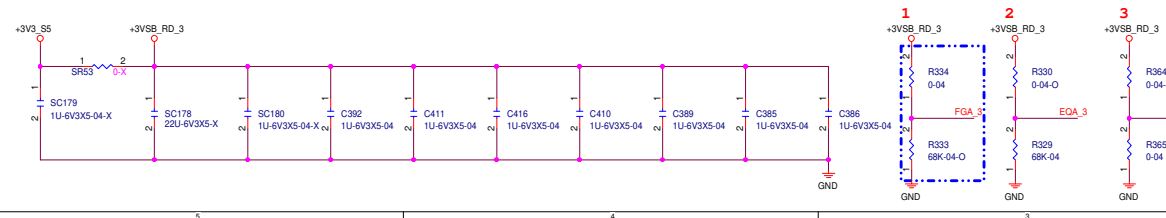


USB3.1 Gen2 Redriver (F_USB31_1)



FGA/B/C/D	Flat Gain Settings (dB)
L (Tie 0-Ω to GND)	-1.2
R (Tie Rext to GND)	0
F (Leave Open)	+1.0 (Default)
H (Tie 0-Ω to VDD)	+2.0

EQA/B/C/D	Equalizer Setting (dB)	
	@2.5 GHz	@5 GHz
L (Tie 0-Ω to GND)	5.0	11.5
R (Tie Rext to GND)	2.7	7.4
F (Leave Open)	4.0	9.9 (Default)
H (Tie 0-Ω to VDD)	6.5	13.1



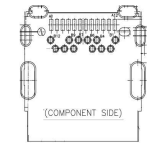
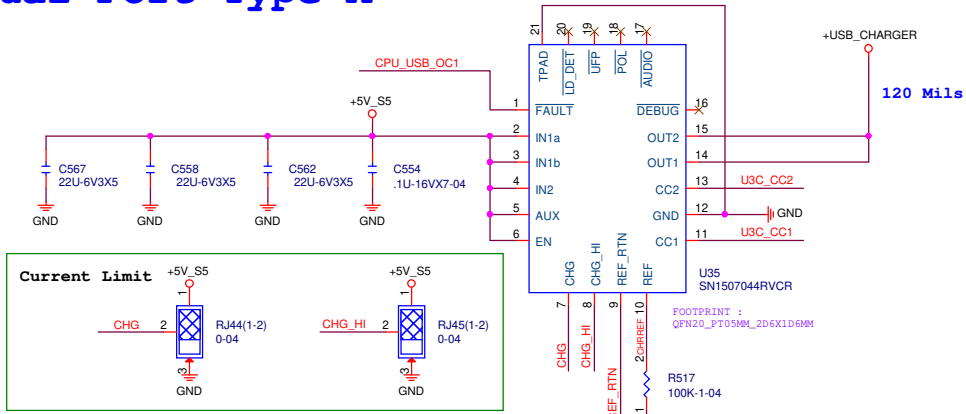
USB3.1 Gen1 Type-C Connector
Co-lay USB3.1 Gen1 Dual Port Type-A

Table 3. USB Type-C Current Advertisement

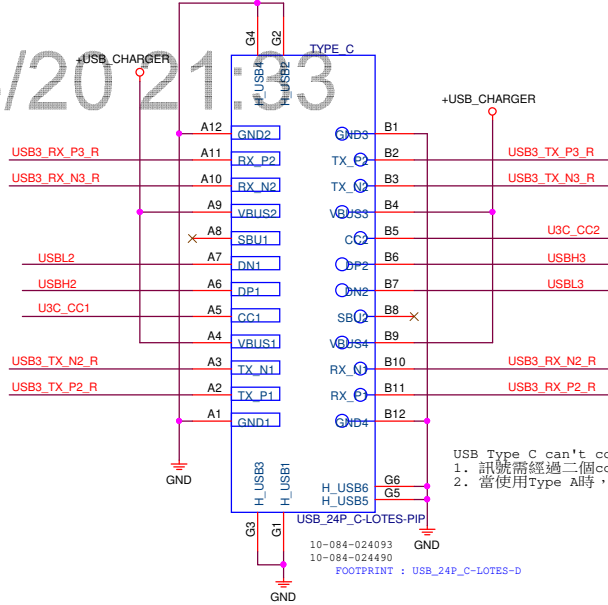
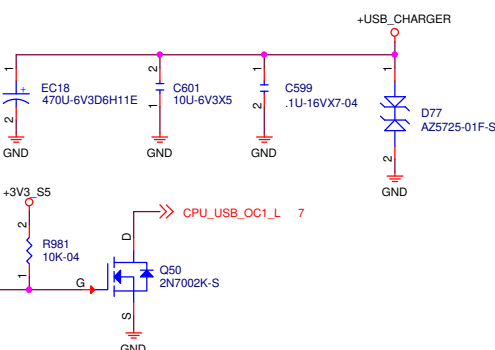
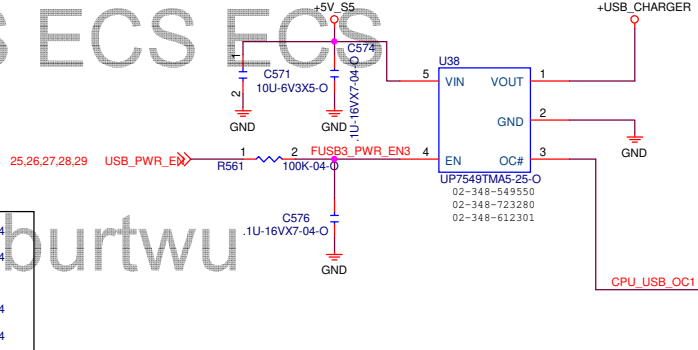
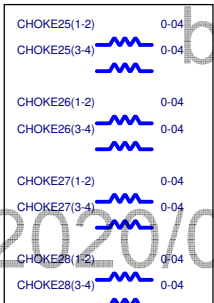
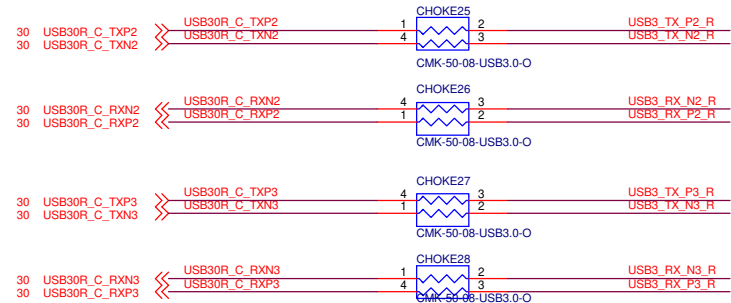
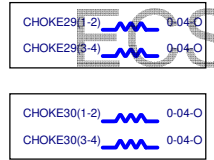
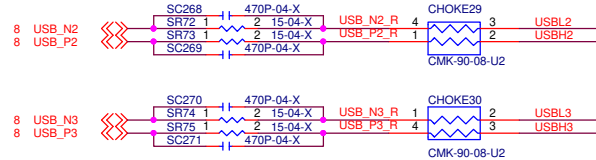
CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

USB Type-C Pin Assignments

No.	Pin Number	Signal Name	No.	Pin Number	Signal Name
1	A1	GND	13	B12	GND
2	A2	SSTxp1	14	B11	SSRxp1
3	A3	SSTxn1	15	B10	SSRxn1
4	A4	Vbus	16	B9	Vbus
5	A5	CC1	17	B8	SBU2
6	A6	Dp1	18	B7	Dn2
7	A7	Dn1	19	B6	Dp2
8	A8	SBU1	20	B5	CC2
9	A9	Vbus	21	B4	Vbus
10	A10	SSRxn2	22	B3	SSTxn2
11	A11	SSRxp2	23	B2	SSTxp2
12	A12	GND	24	B1	GND

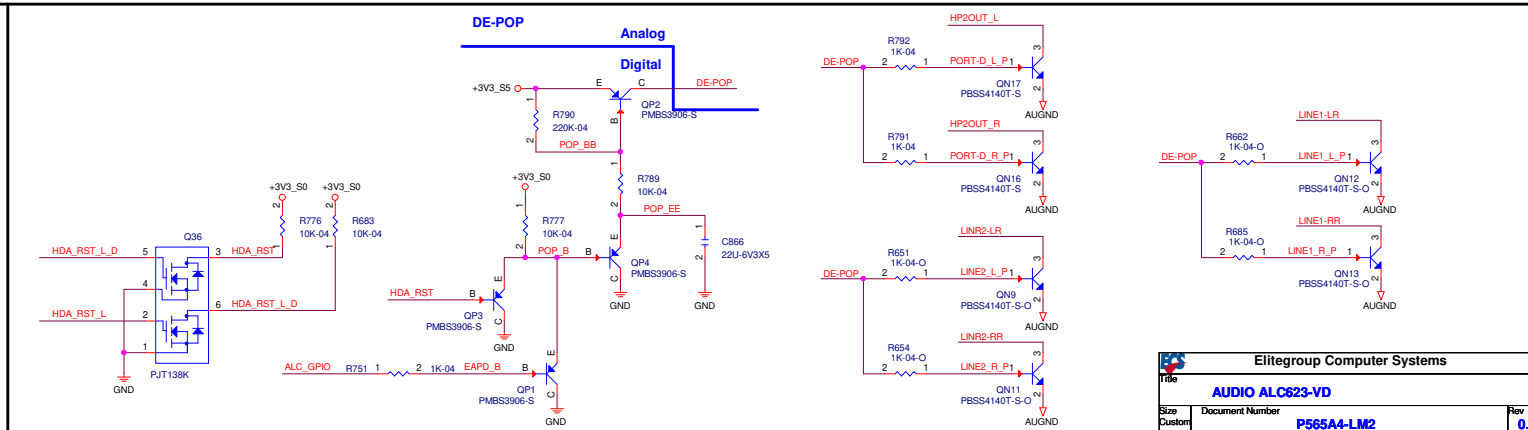
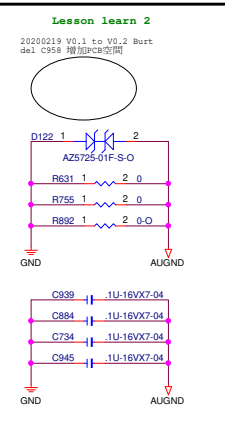
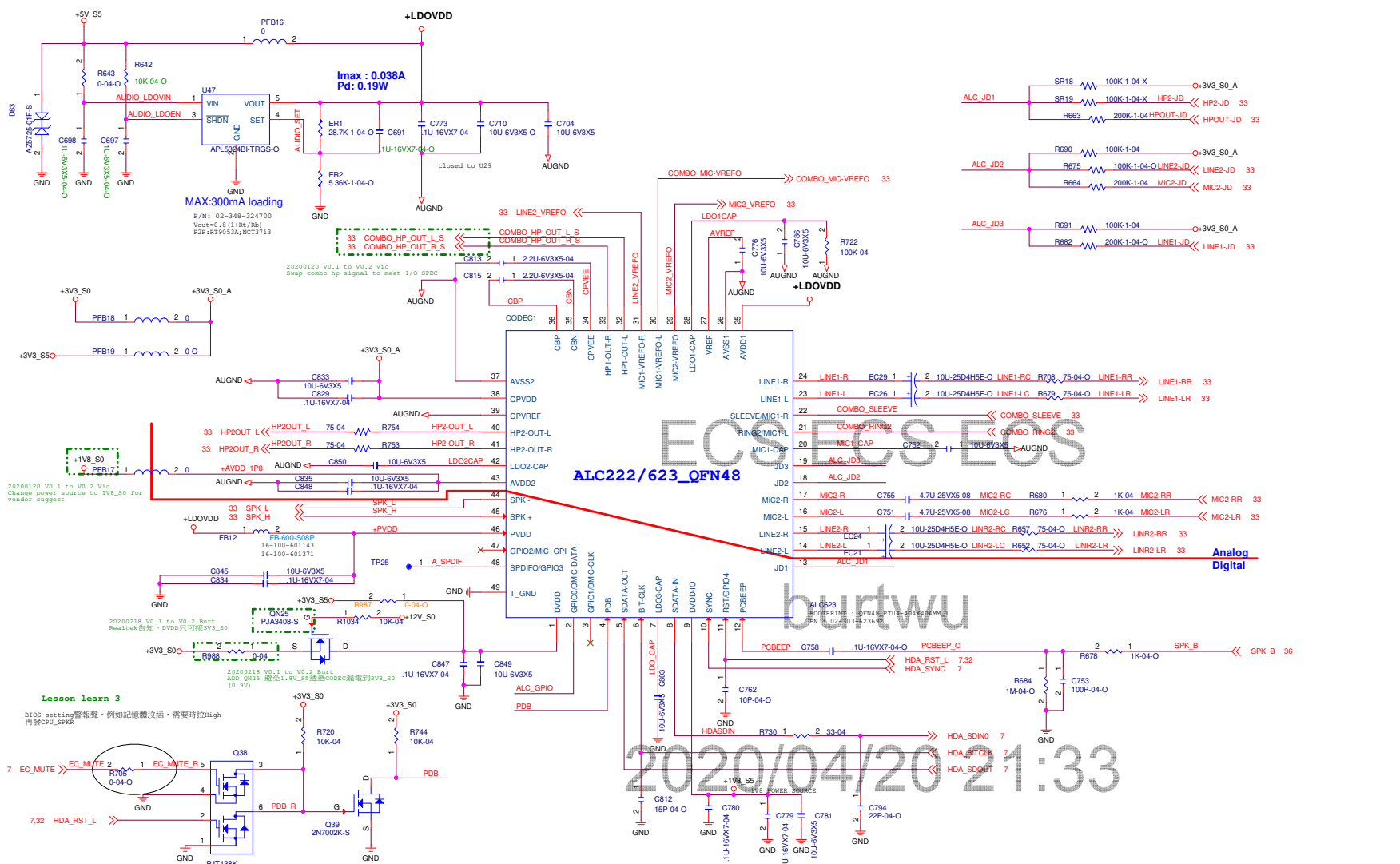


CPU USB3.0 port_2 /USB 2.0 port_2
CPU USB3.0 port_3 /USB 2.0 port_3

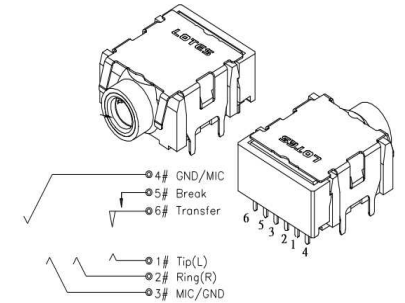
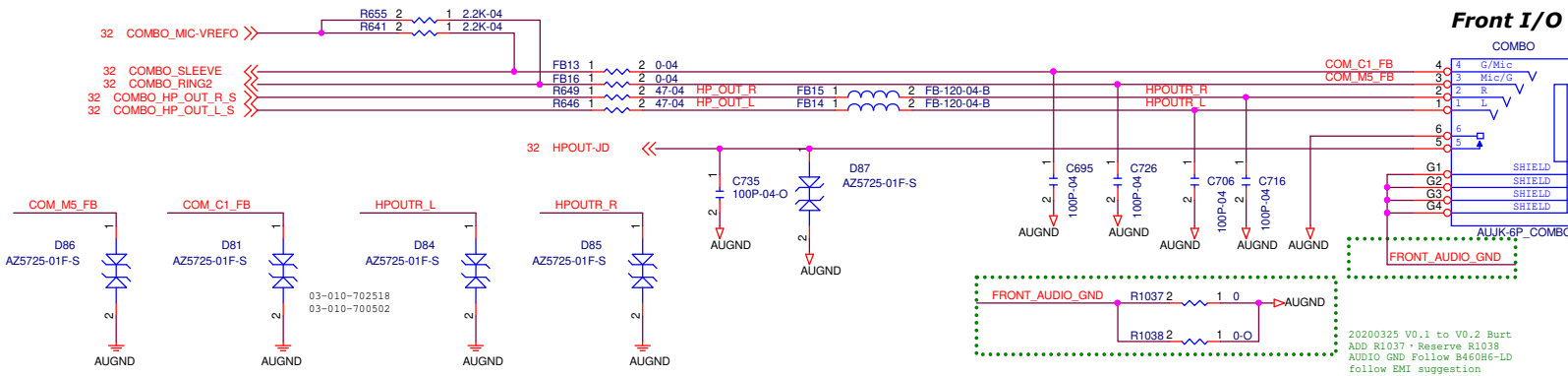


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USB Type C can't colay Type A
1. 訊號需經過二個connector會有阻抗不匹配問題。
2. 當使用Type A時，延伸到Type C的Trace會變成Stub。

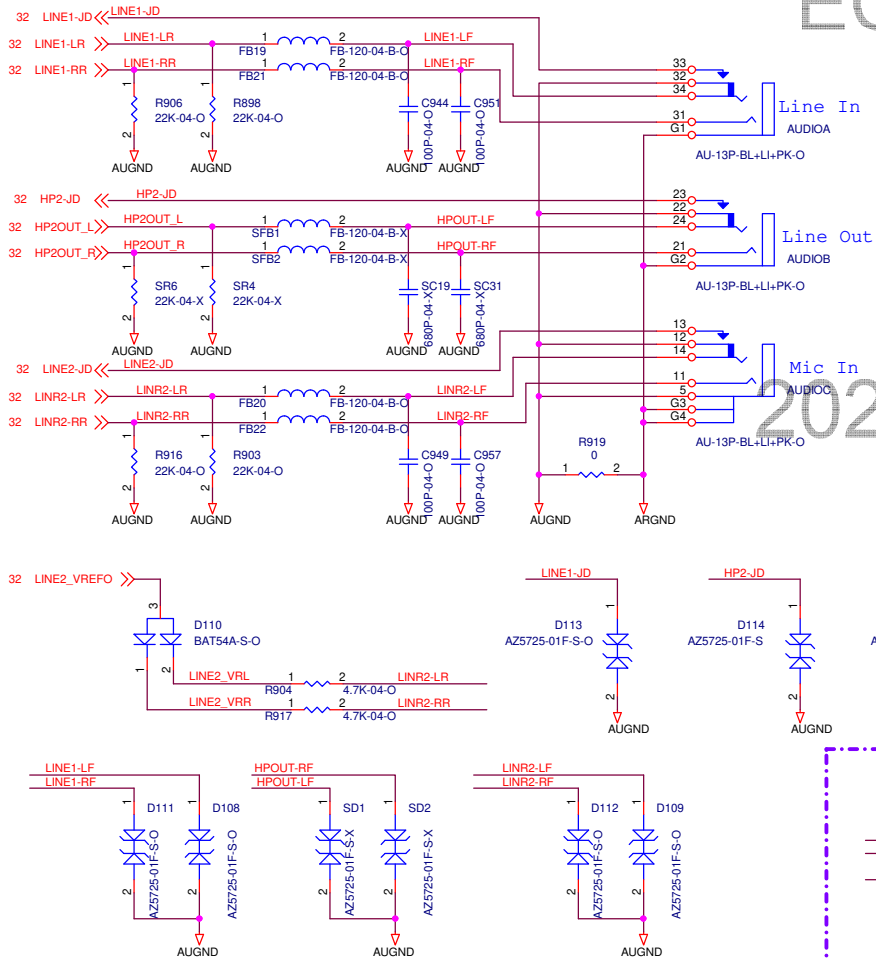


COMBO Audio Jack

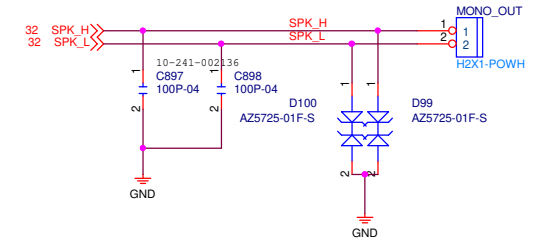


footprint : AUDIO_JACK_6P-LOTES-PIP-A
Can be Support NOKIA/APPLE HP

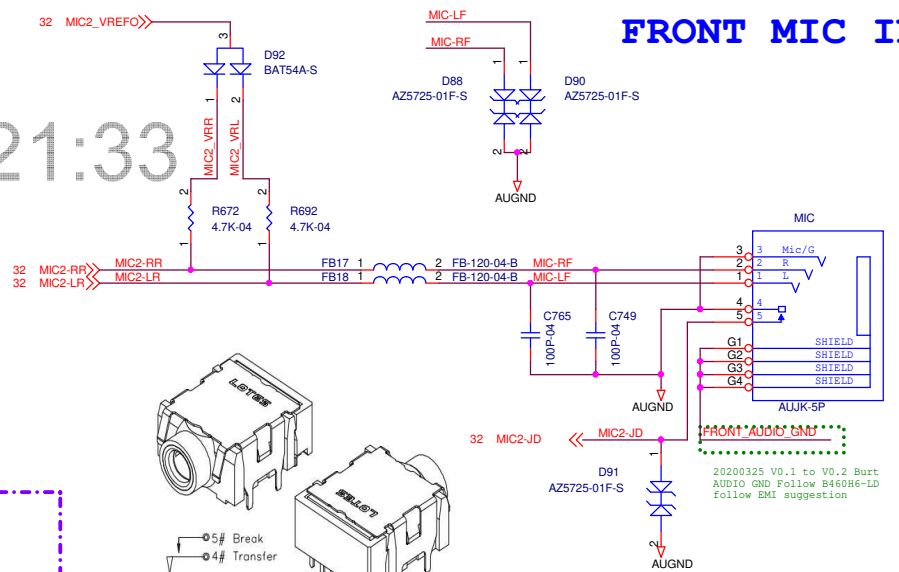
REAR I/O 5.1 CH



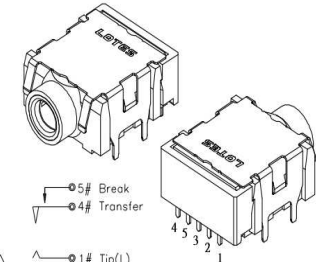
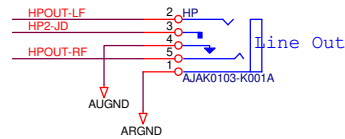
MONO Amplifier

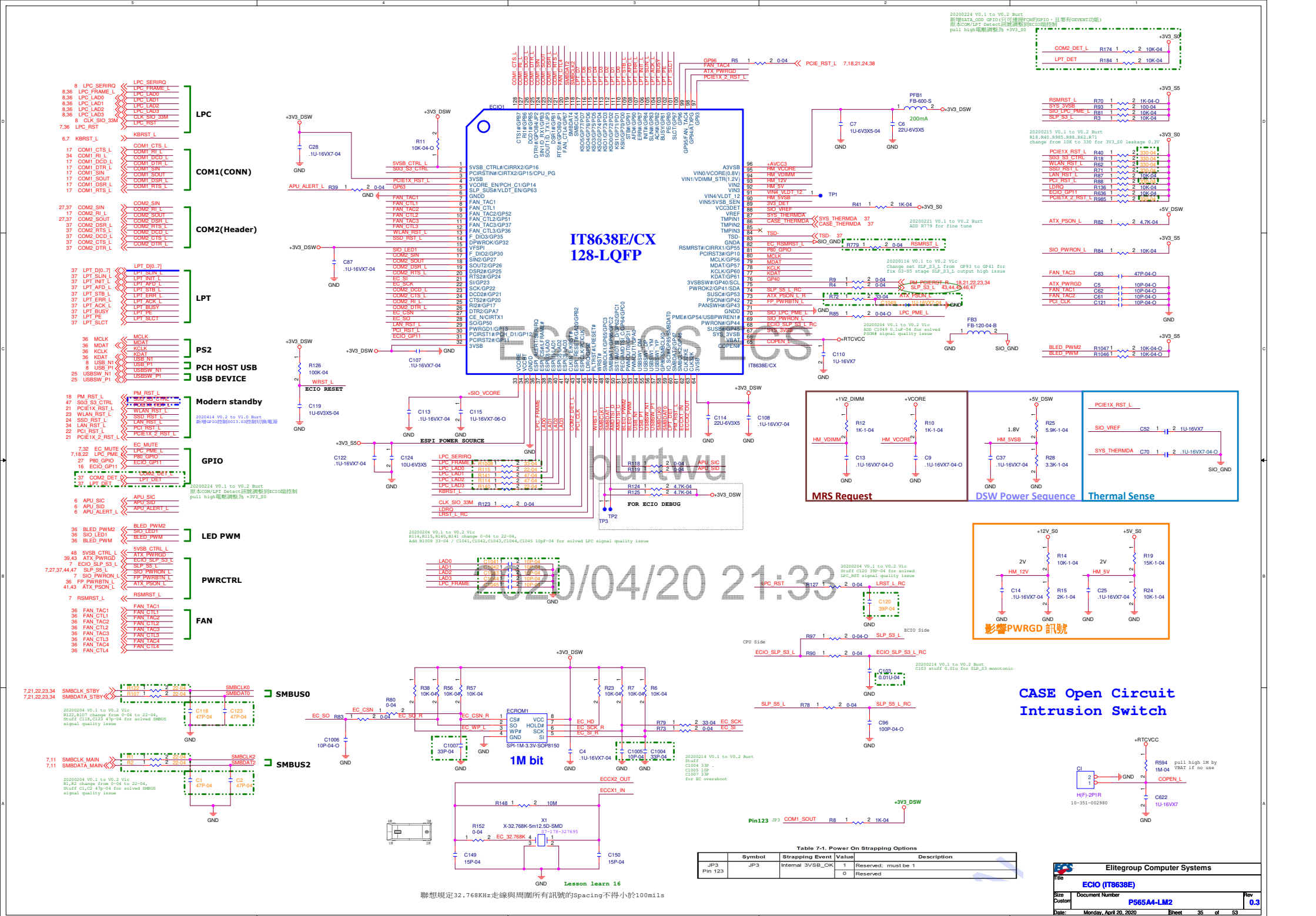


FRONT MIC IN

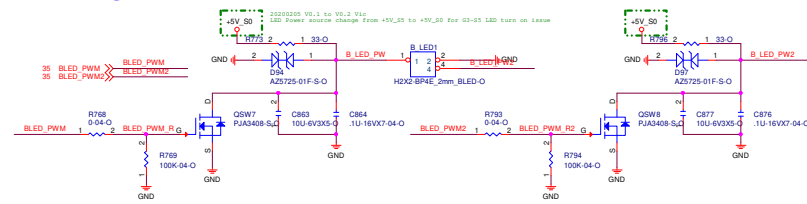


REAR HP OUT

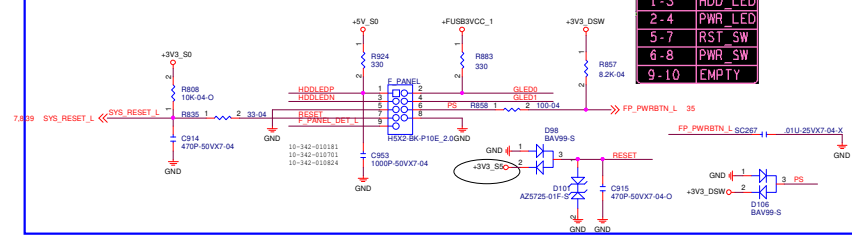




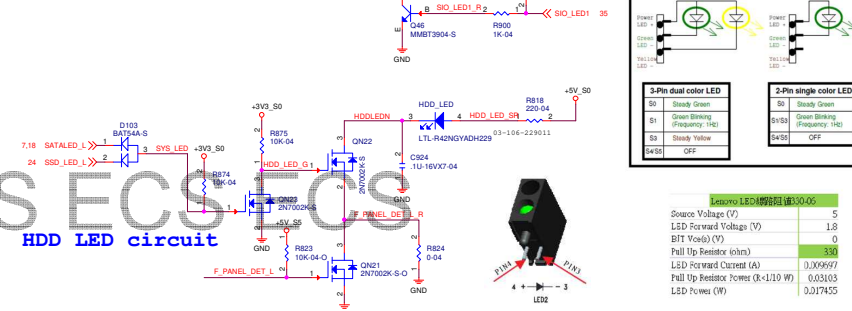
Breathing LED header



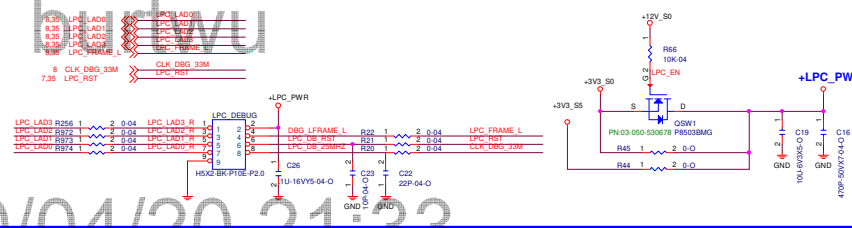
Front Panel



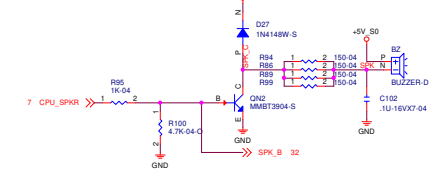
Power LED circuit (single color LED)



LPC DEBUG PORT

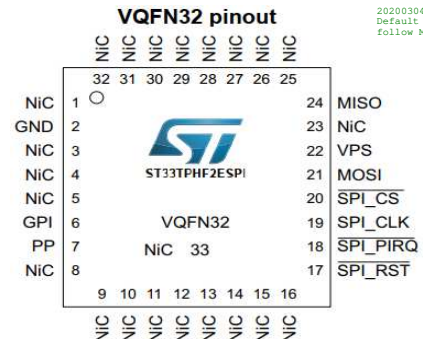
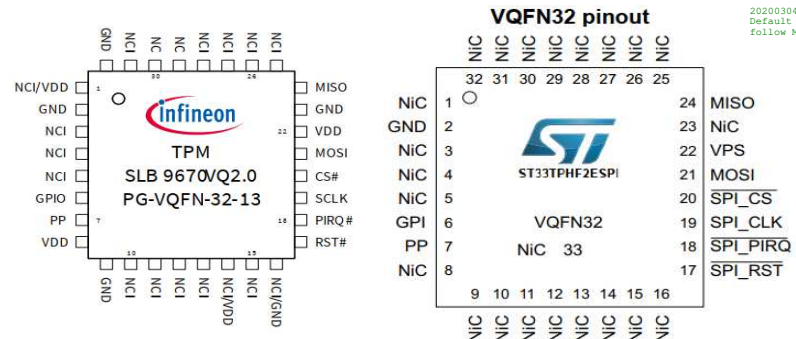
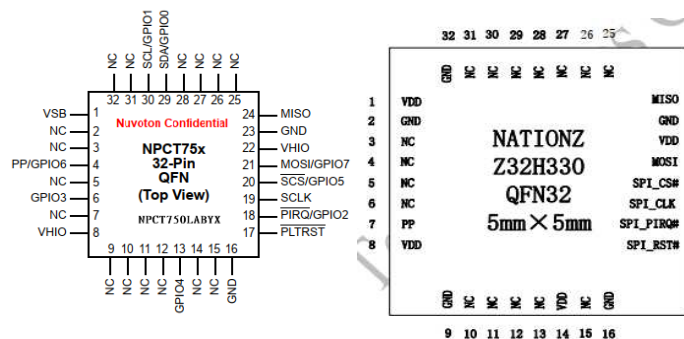
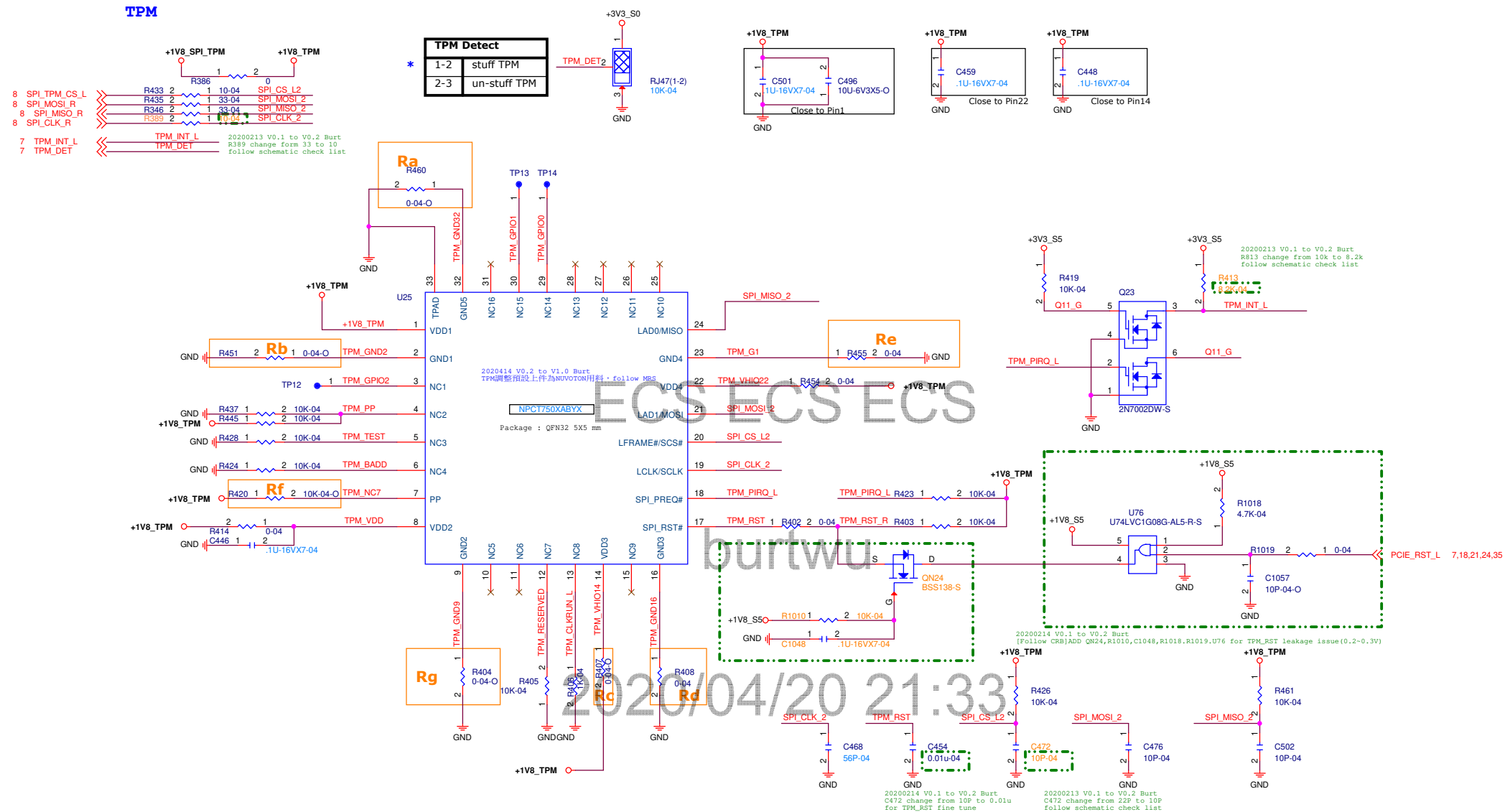


Buzzer



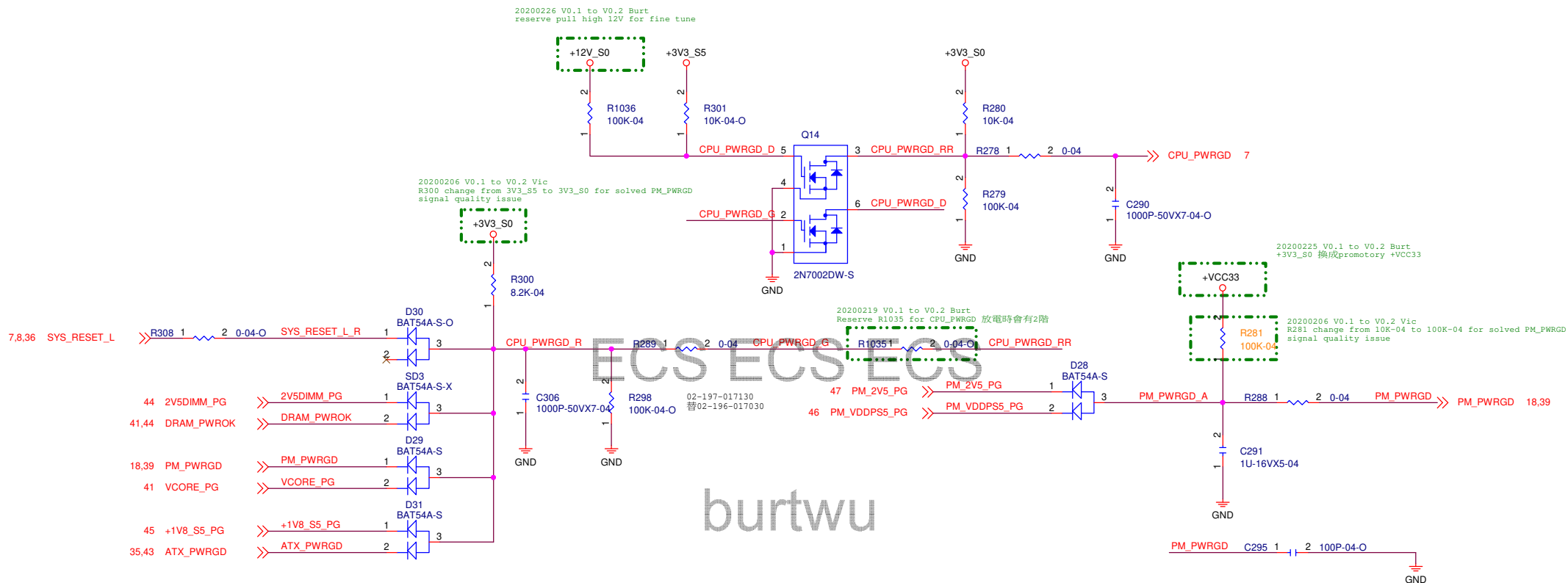
KB/MS Conn





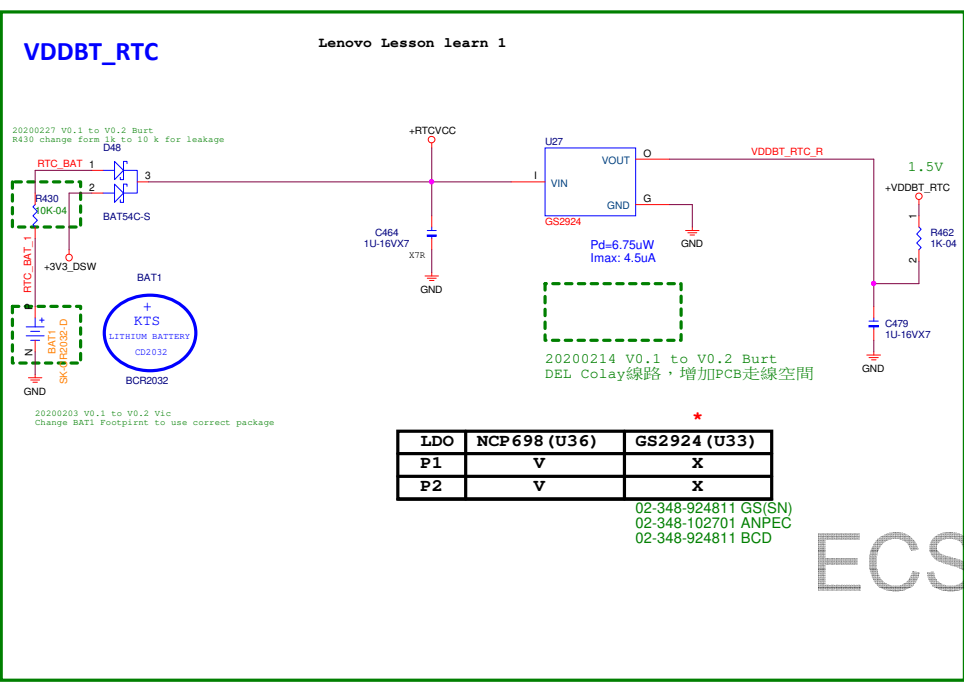
TPM 2.0(SPI interface)

	Ra	Rb	Rc	Rd	Re	Rf	Rg
NATIONZ	V	V	V	V	V	V	V
Nuvoton	X	X	X	V	V	X	X
Infineon	V	V	X	X	V	X	V
ST	X	V	X	X	X	V	X



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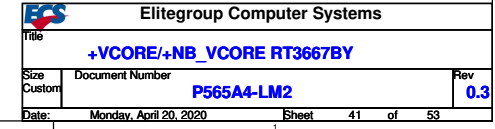
Elitegroup Computer Systems		
Title		
SEQUENCE CIRCUIT		
Size	Document Number	Rev
B	P565A4-LM2	0.3
Date:	Monday, April 20, 2020	Sheet 39 of 53



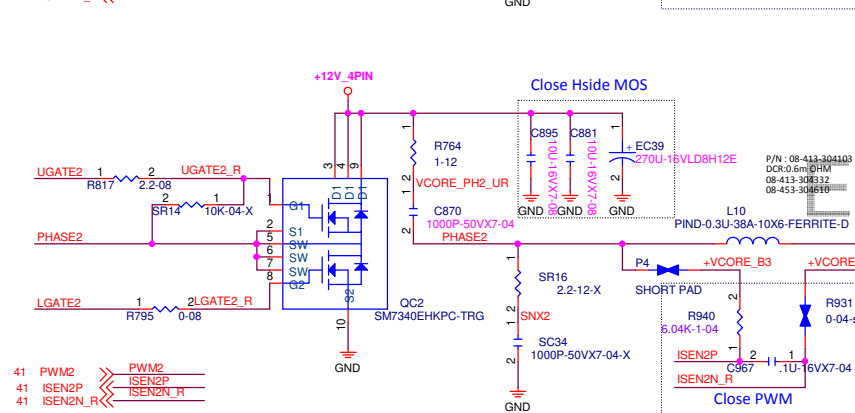
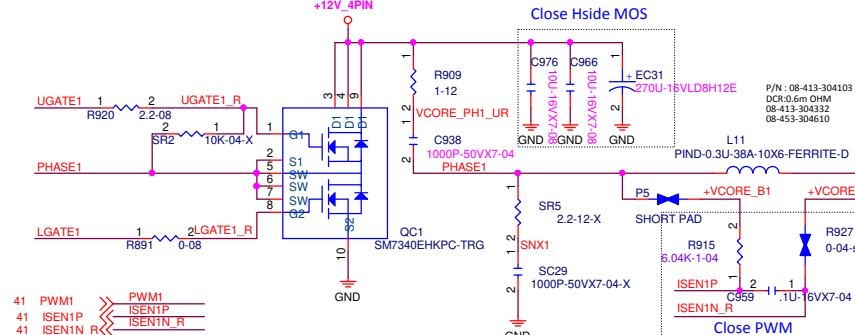
+VDDCR_SOC_S5
不支援BR CPU

burtwu

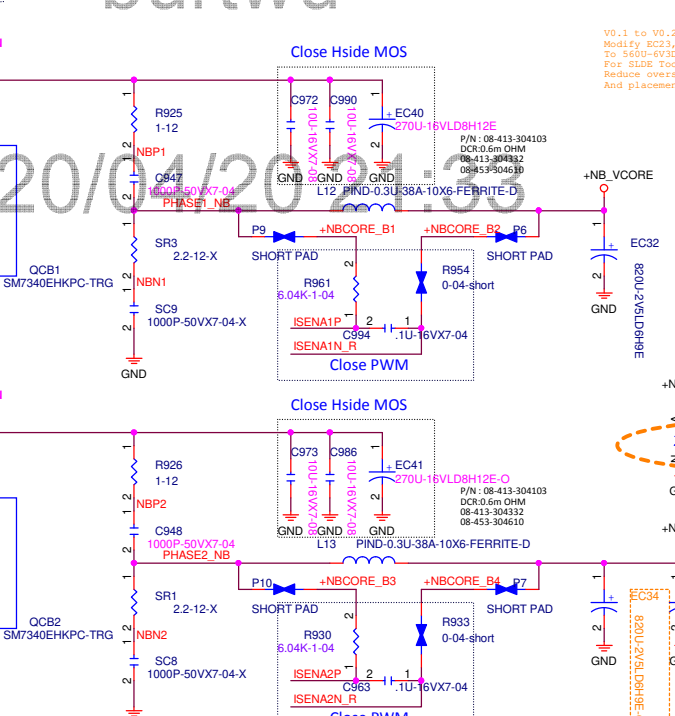
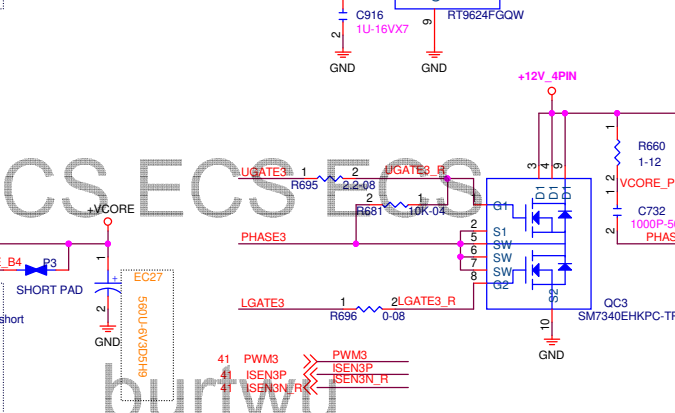
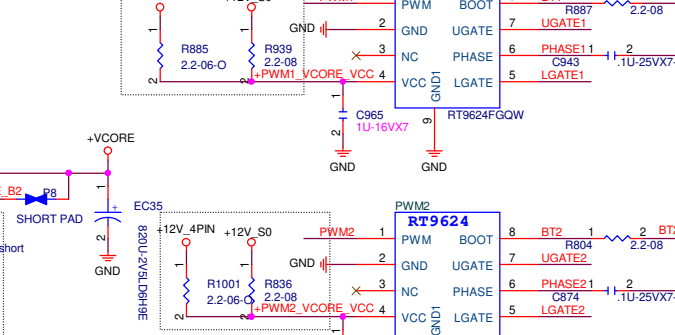
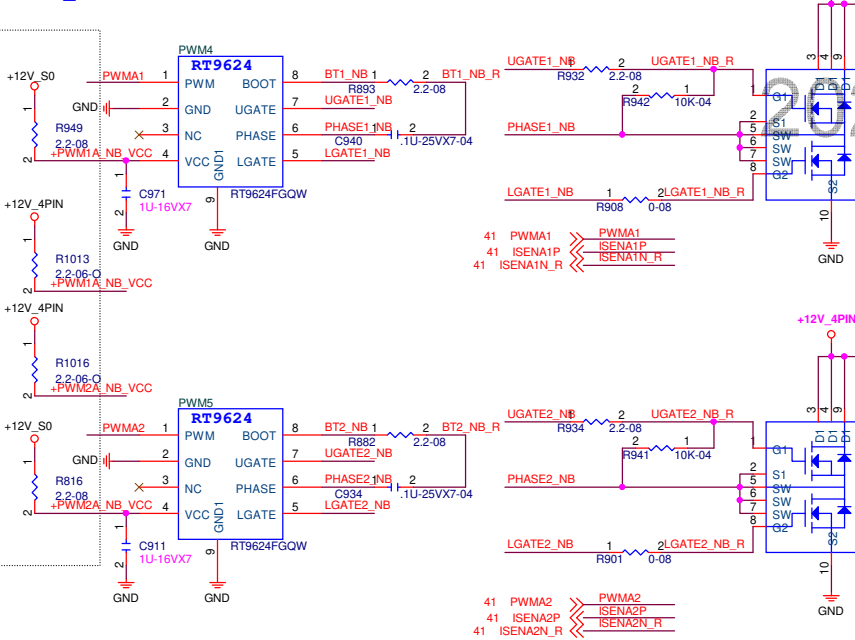
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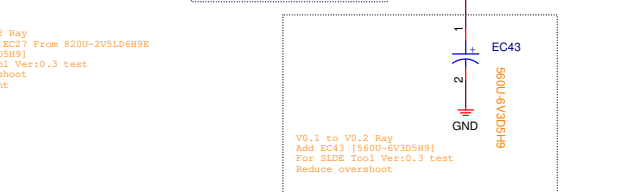
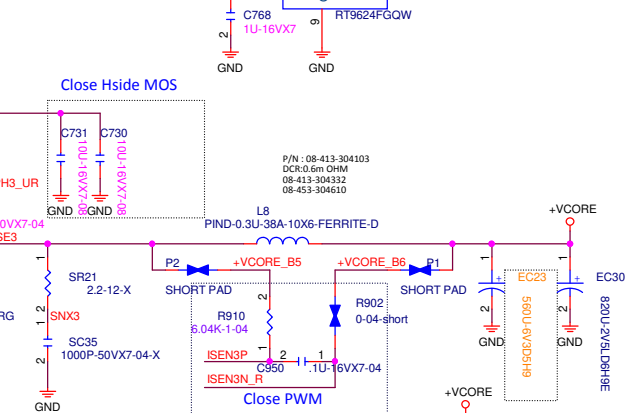
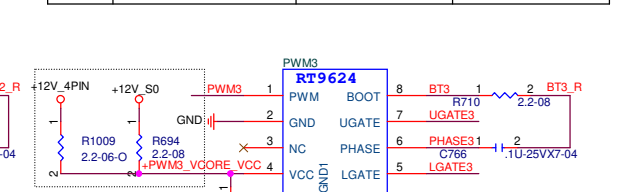
+V CORE



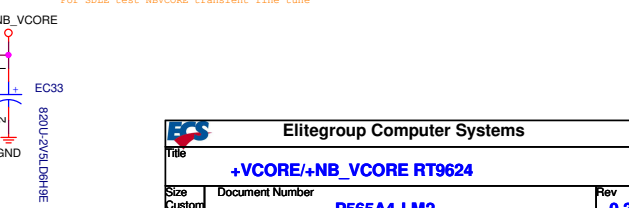
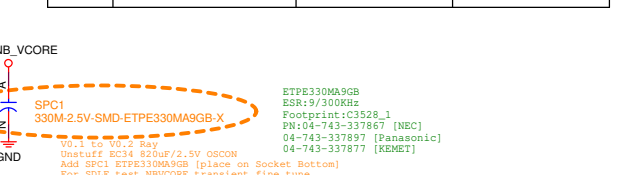
+NB_V CORE



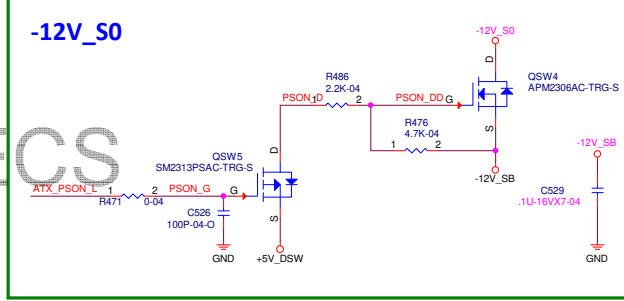
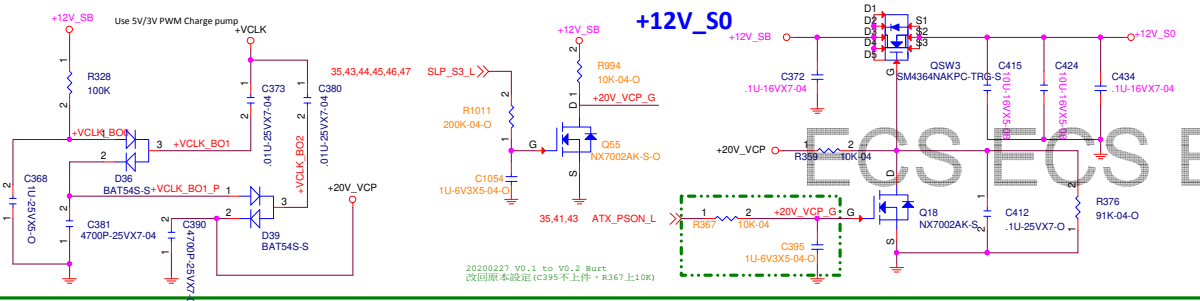
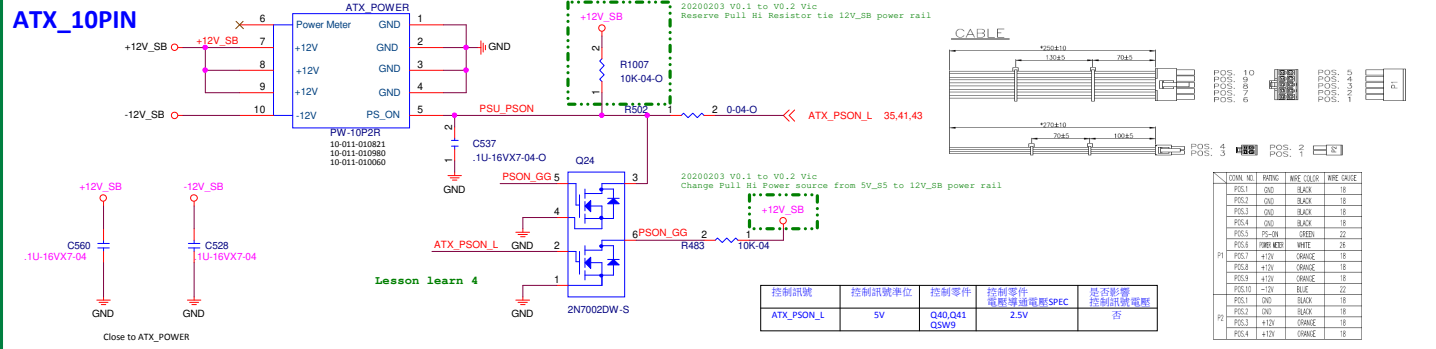
AM4	65W(Matisse) (Vermeer) (Pinnacle Ridge) 不支援内臓	65W(Raven Ridge) (Picasso) (Renior) 支援内臓	35W(Raven Ridge) (Picasso) (Renior) 支援内臓
VCCVID	0.75V~1.5V	0.75V~1.5V	0.75V~1.5V
TDC	60A/OC design:100A	65A/OC design:100A	39A/OC design:100A
EDC	90A/WOC design:130A	95A/WOC design:130A	55A/WOC design:130A



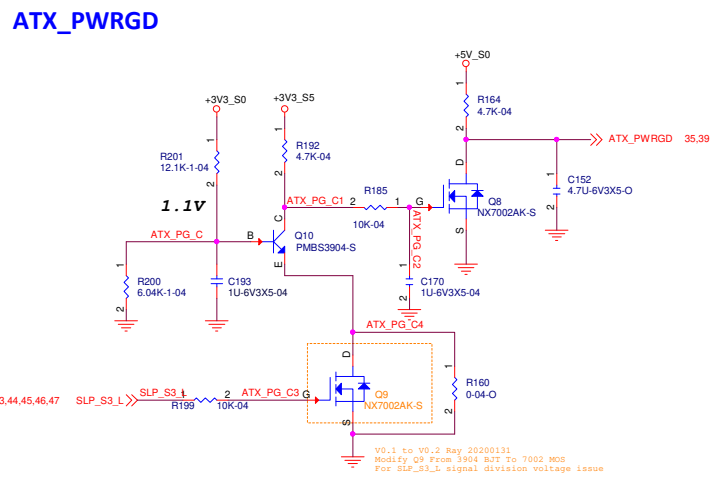
AM4	65W(Matisse) (Vermeer) (Pinnacle Ridge) 不支援内臓	65W(Raven Ridge) (Picasso) (Renior) 支援内臓	35W(Raven Ridge) (Picasso) (Renior) 支援内臓
VCCVID	0.75V~1.2V	0.75V~1.2V	0.75V~1.2V
TDC	30A/OC design:65A	50A/OC design:65A	40A/OC design:65A
EDC	35A/WOC design:90A	75A/WOC design:90A	60A/WOC design:90A



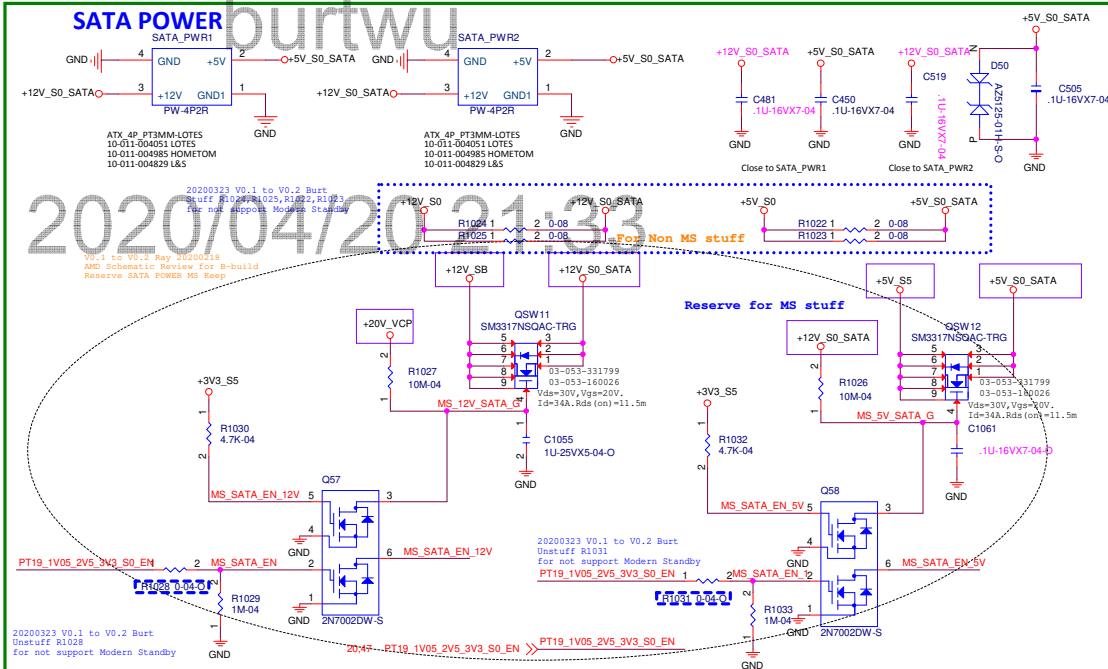
ATX_10PIN



ATX_PWRGD



SATA POWER



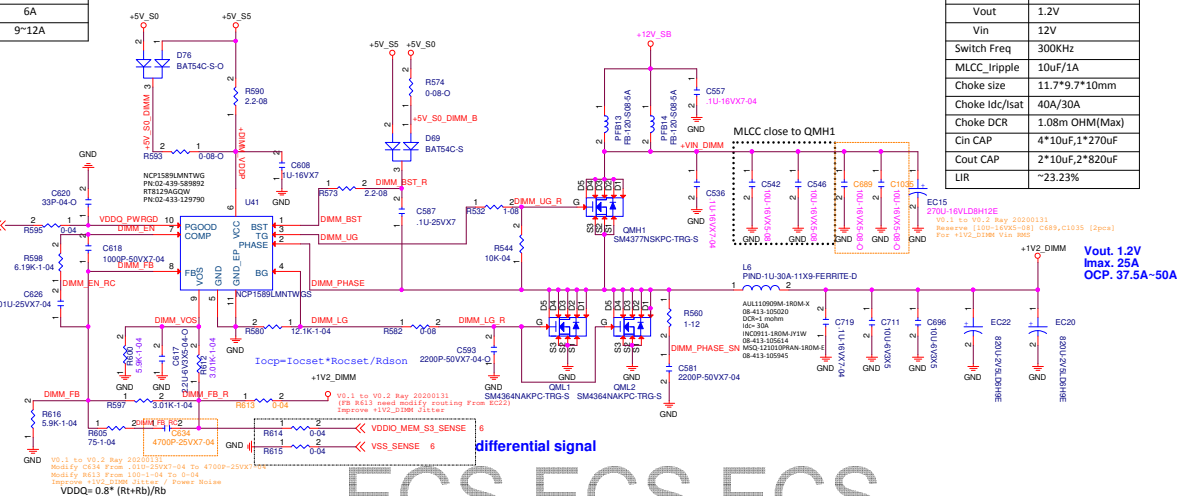
+1V2_DIMM

AM4	65W(Matisse) (Vermore) (Pinnacle Ridge)	65W(Raven Ridge) (Picasso) (Renoir) 支援內顯	35W(Raven Ridge) (Picasso) (Renoir) 支援內顯
Voltage	1.2V	1.2V	1.2V
TDC	15.5A	6A	6A
IOCP	23.25~31A	9~12A	9~12A

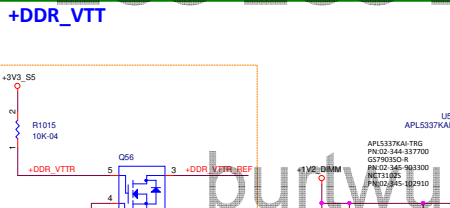
STATE	S3	SS	VRDDQ	VTT
Hi	Hi	Hi	on	on
Lo	Lo	Lo	off	off

EN(vb)	NCP1589LMNTWGS
Hi	>0.8V
Low	<0.3V

EN(vb)	RT8129AGQW
Hi	>0.8V
Low	<0.8V

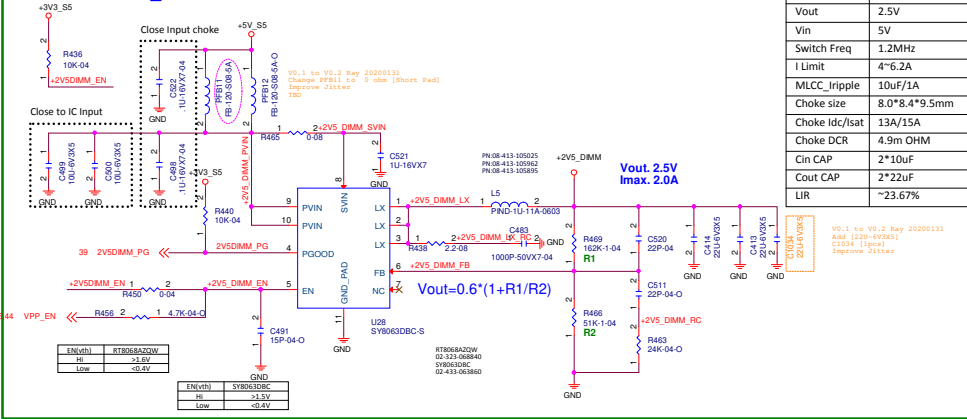


FCS FCS FCS

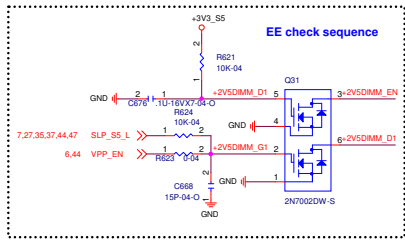
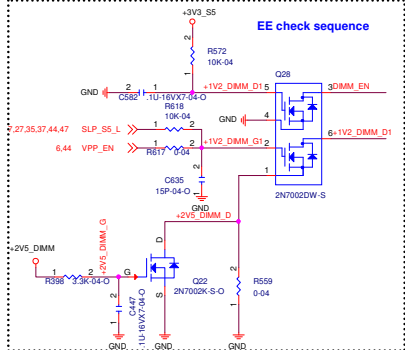


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+2V5_DIMM

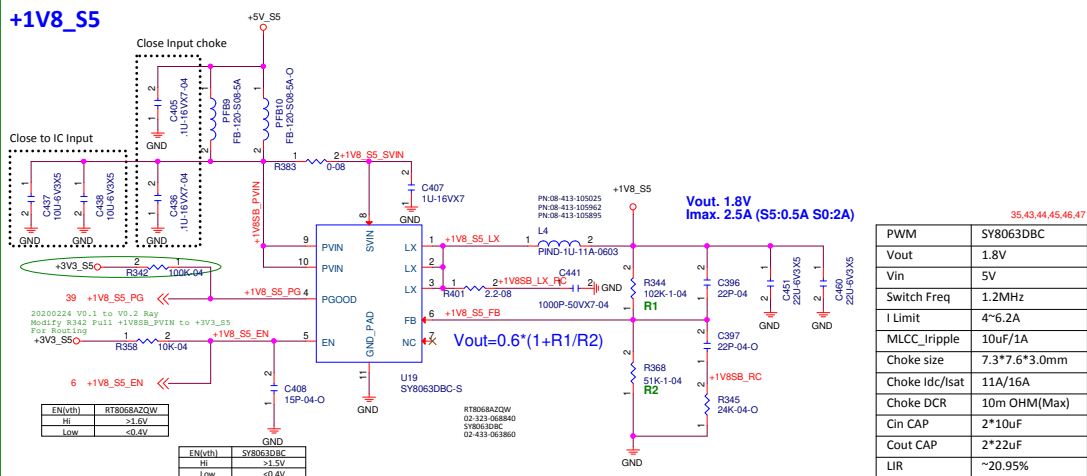


LDO	APL5337KAI-TRG
IMAX	1.5A
Vout	0.6V
Vin	1.2V
I Limit	2A
Cin CAP	1*10uF
Cout CAP	2*10uF
JA	55°C/W
Pd	0.9W

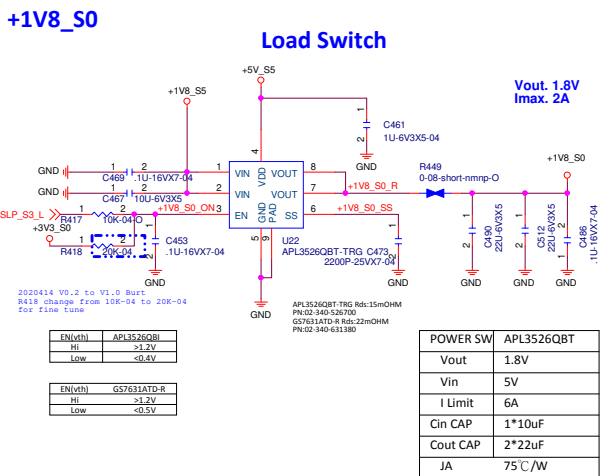


控制訊號	控制訊號單位	控制零件	控制零件	控制零件
SLP_SS_L	3.3V	Q31,Q32	2.5V	控制訊號電壓SPIC

+1V8_S5

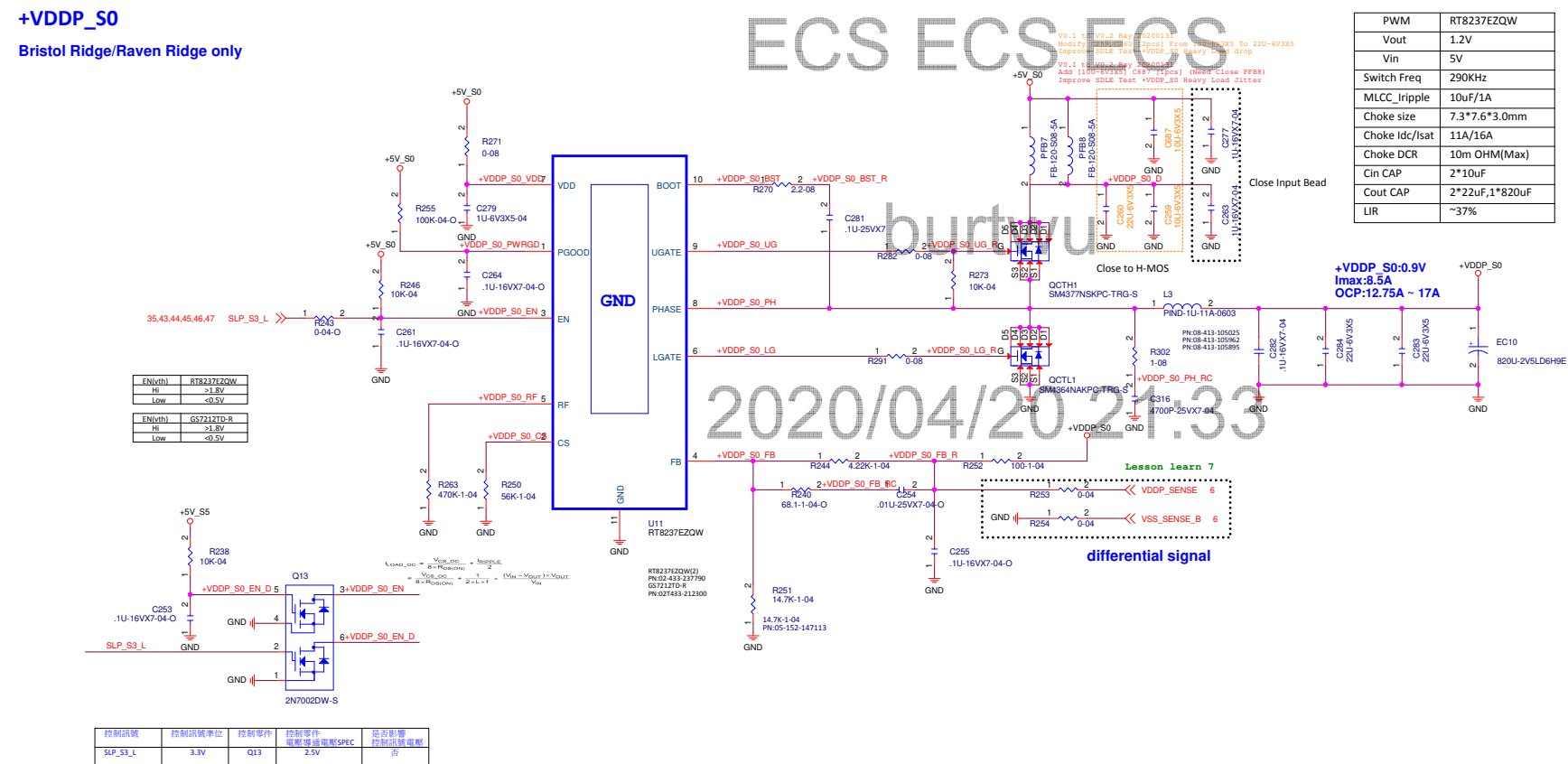


+1V8_S0



+VDDP_S0

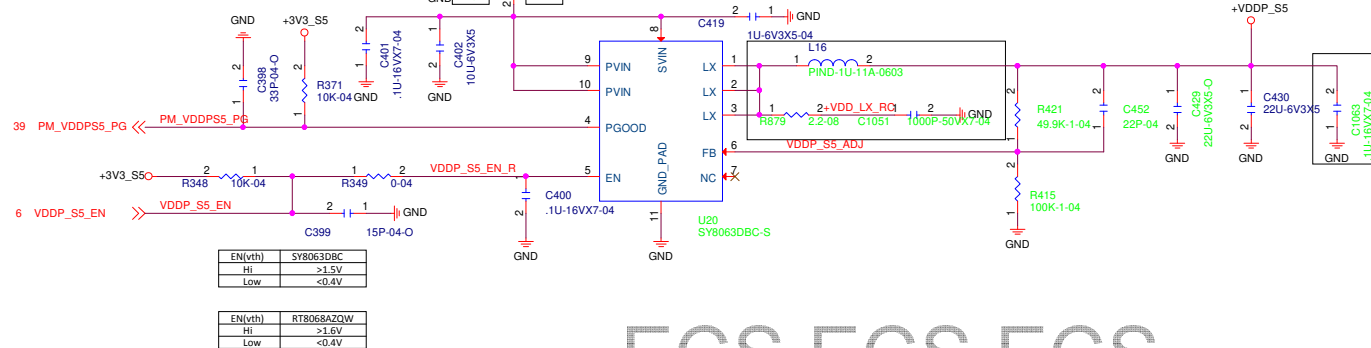
Bristol Ridge/Raven Ridge only



+VDDP_S5

20200224 V0.1 to V0.2 Ray
Modify U20 LDO [APL5934C] To Converter [RT8068]
Improve S5 power consumption.

Vout=0.9V
Imax. 1A



PWM	SY8063DBC
Vout	0.9V
Vin	5V
Switch Freq	1.2MHz
I Limit	4~6.2A
MLCC_ripple	10uF/1A
Choke size	7.3*7.6*3.0mm
Choke Idc/Isat	11A/16A
Choke DCR	10m OHM(Max)
Cin CAP	1*10uF
Cout CAP	2*22uF
LIR	~20.95%

+VDD_FCH

20200220 V0.1 to V0.2 Ray
Modify U8 RT7238 to LV7298AHGQW [TPS54623
For RT popular converter solution.

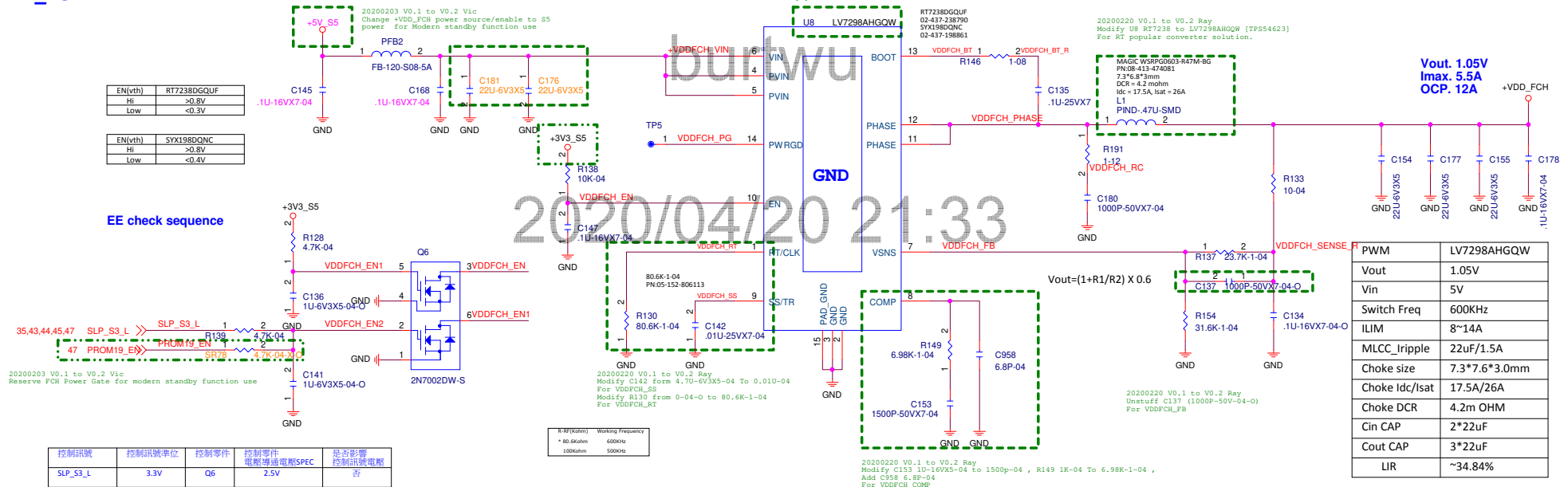
```
20200203 V0.1 to V0.2 Vic
Change +VDD_FCH power source/enable to S5
power for Modern standby function use
```

20200220 V0.1 to V0.2 Ray
Modify U8 RT7238 to LV7298AHGQW [TPS54623]
For RT popular converter solution.

EN(vth)	RT7238DGQUF
Hi	>0.8V
Low	<0.3V

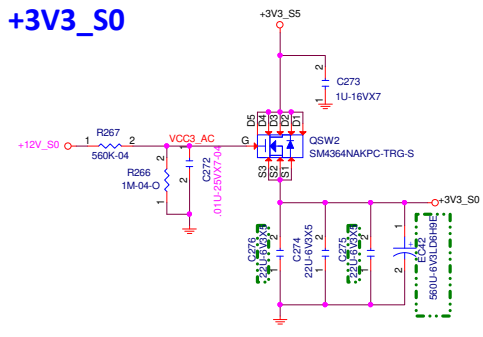
EN(vth)	SYX198DQNC
Hi	>0.8V
Low	<0.4V

EE check sequence



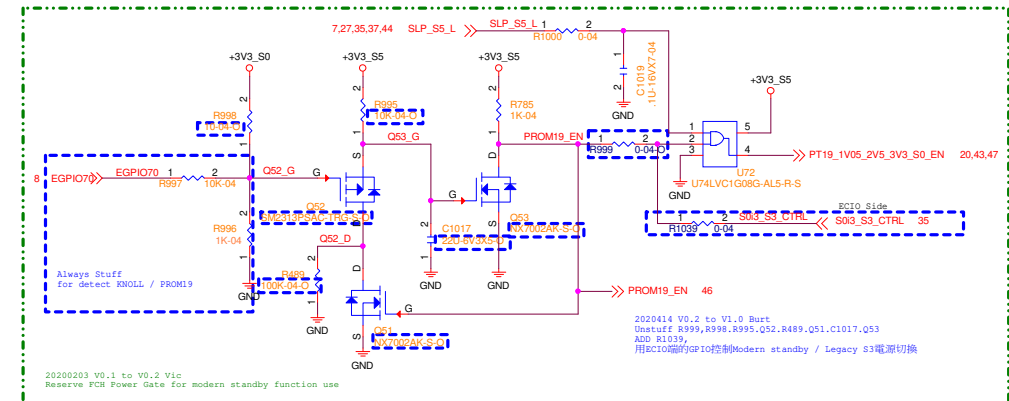
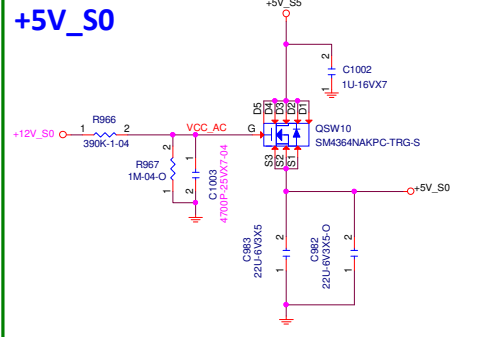
SE-4-O	PWM	LV7298AHQGW
	Vout	1.05V
	Vin	5V
	Switch Freq	600KHz
	ILIM	8~14A
	MLCC_ripple	22uF/1.5A
	Choke size	7.3*7.6*3.0mm
	Choke Idc/Isat	17.5A/26A
	Choke DCR	4.2m OHM
	Cin CAP	2*22uF
Cout CAP	3*22uF	
LIR	~34.84%	

+3V3_S0



20200215 V0.1 to V0.2 Burt
ADD EC42
Stuff C275, C276
for VGA Power Noise fall

+5V_S0



20200203 V0.1 to V0.2 Vic
Reserve FCH Power Gate for modern standby function use

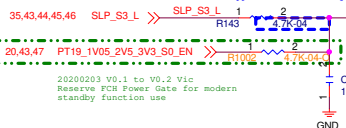
+2V5_FCH

控制訊號	控制訊號單位	控制零件	控制零件 電阻/電容/電壓/SPEC	是否影響 控制訊號電壓
SLP_S3_L	3.3V	Q5	2.5V	否

39 PM_2V5_PG

EE check sequence

20200323 V0.1 to V0.2 Burt
Unstuff R1002
Stuff R1043
For not support Modern Standby



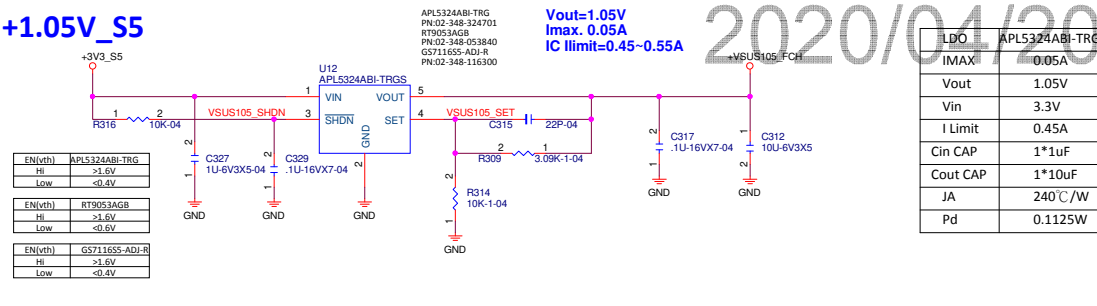
20200203 V0.1 to V0.2 Vic
Change +2V5_FCH power source/enable to S5 power
for Modern standby function use

EN(vth)	RT9059AGQW	EN(vth)	APL5934CQBI-TRGS	EN(vth)	G571665D-R
Hi	>1.2V	Hi	>1.1V	Hi	>1.2V
Low	<0.4V	Low	<0.5V	Low	<0.6V

Vout=2.5V
Imax. 0.9A

LDO	RT9059AGQW
IMAX	1A
Vout	2.5V
Vin	3.3V
I Limit	3.1A
Cin CAP	1*10uF
Cout CAP	2*22uF
JA	75°C/W
Pd	0.8W

+1.05V_S5



Vout=1.05V
Imax. 0.05A
IC Ilimit=0.45~0.55A

LDO	APL5324ABI-TRGS
IMAX	0.05A
Vout	1.05V
Vin	3.3V
I Limit	0.45A
Cin CAP	1*1uF
Cout CAP	1*10uF
JA	240°C/W
Pd	0.1125W

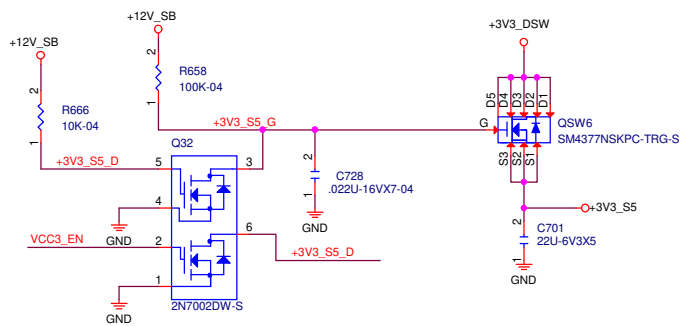
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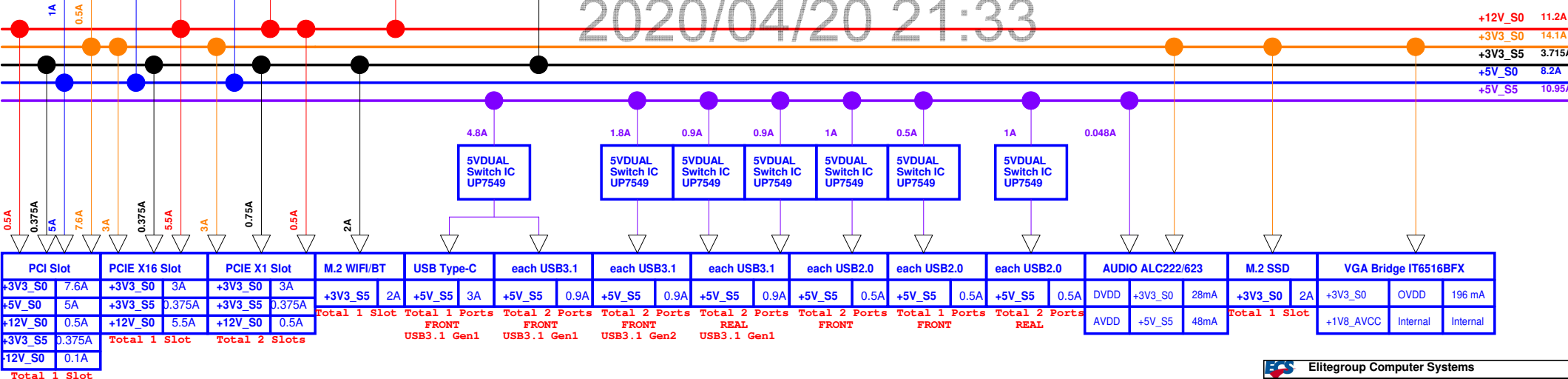
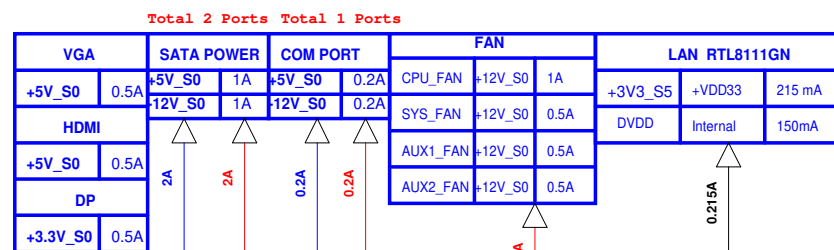
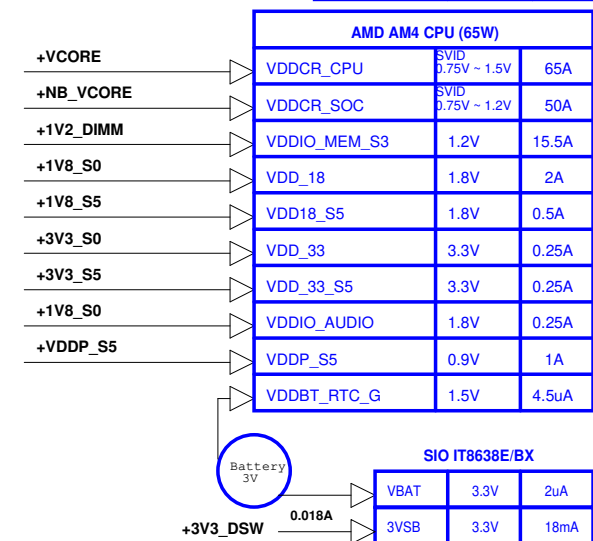
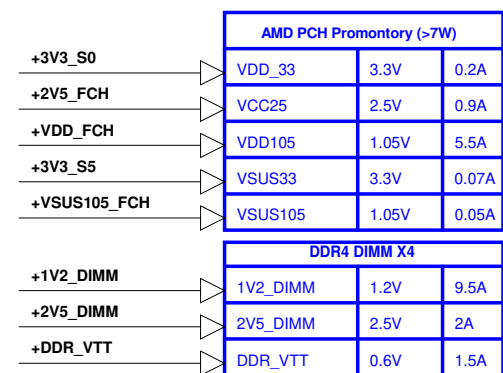
Elitegroup Computer Systems			
Title	VCC/VCC3/+1.05V_S5/+2V5_FCH		
Size	Document Number	P565A4-LM2	Rev
Custom			0.3
Date	Monday, April 20, 2020	Sheet	47 of 53

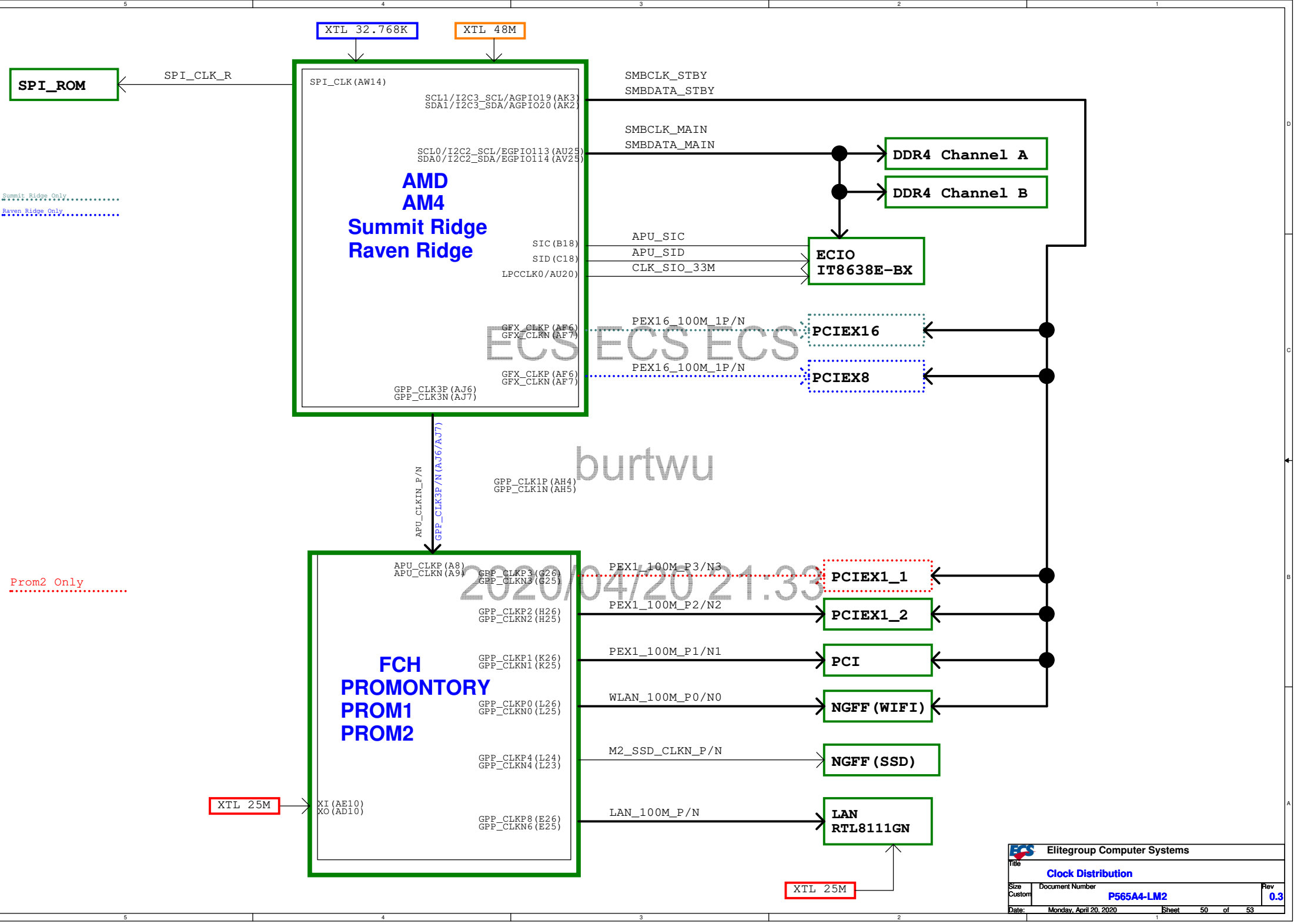
EN(Vth)	GS7225BTQ-R
Hi	>1.6V
Low	<0.4V

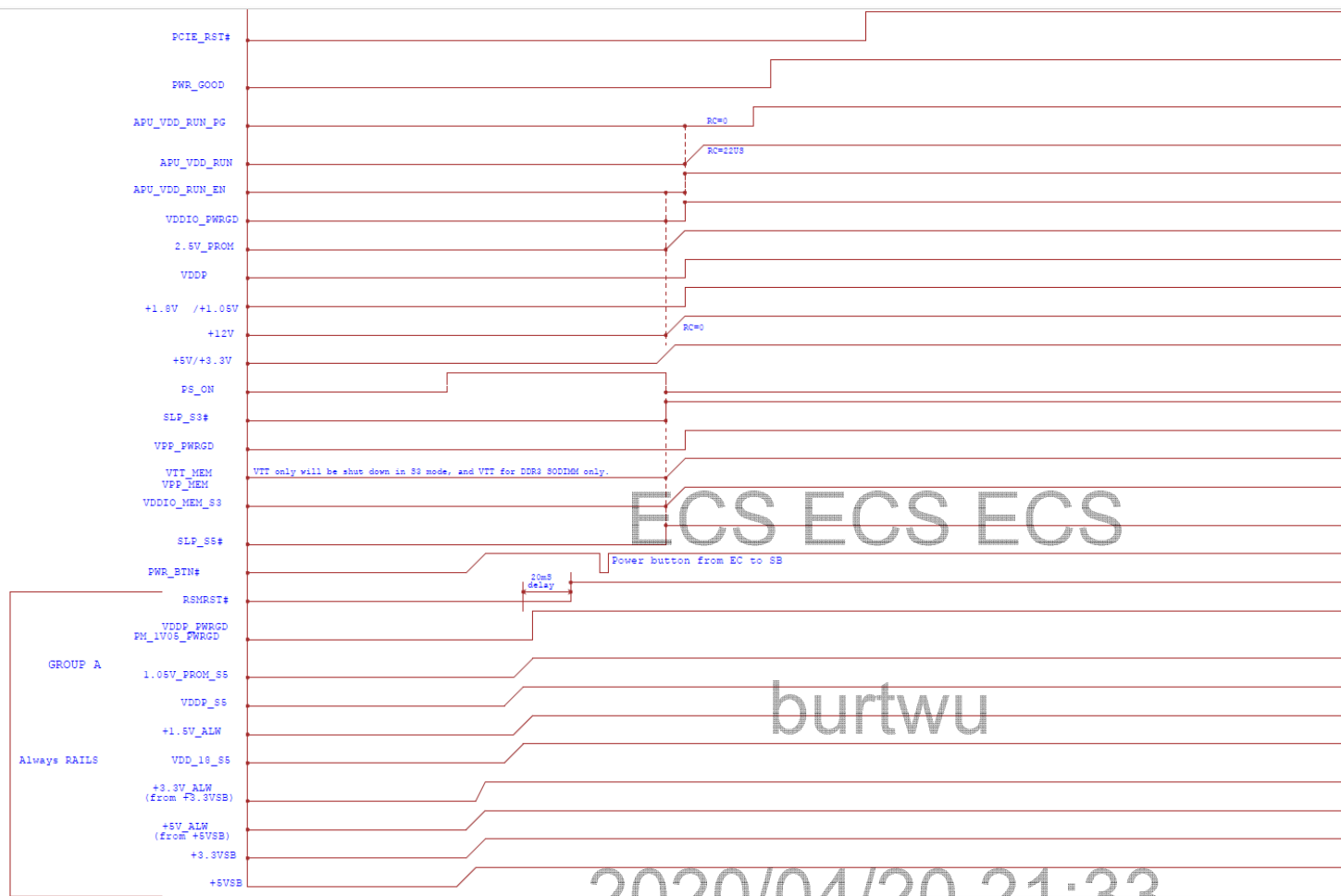


PWM	RT6576DGQW	PWM	RT6576DGQW
Vout	5V	Vout	3.3V
Vin	12V	Vin	12V
Switch Freq	300KHz	Switch Freq	355KHz
IOCP	27~36A	IOCP	27~36A
MLCC_ripple	1A*2	MLCC_ripple	1A*2
Choke size	10.8*10.8*10.3mm	Choke size	10.8*10.8*10.3mm
Choke Idc/Isat	20A/25A	Choke Idc/Isat	20A/25A
Choke DCR	2.9m OHM	Choke DCR	2.9m OHM
Cin CAP	3*10uF, 1*270uF	Cin CAP	3*10uF
Cout CAP	2*22uF, 1*560uF	Cout CAP	2*22uF, 1*560uF
LIR	~24.55%	LIR	~20%









2020/04/20 21:33

Table 60. AM4 Power Sequencing Group Definitions with coin cell battery

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_SOC_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_SOC, VDDCR_CPU,

ECIO-GPIO function

Data:2019/12/03

Pin Name	Power Well	Usage	Default SET	Boot Set(BIOS Check)
Pin 7/9/11/99		FAN_TAC	FAN_TAC	FAN_TAC
Pin 8/10/12/120		FAN_CTL	FAN_CTL	FAN_CTL
F_DIO3/GP35		WLAN_RST_L	GP35	S3/S5 GPO High ,S0 GPO Low
DPWROK/GP32		SSD_RST_L	GP32	S3/S5 GPO High ,S0 GPO Low
F_DIO2/GP30		SIO_LED1	PWM	S5 GPO Low ,S3 GPO 1KHz,S0 GPO High
Pin 17~20,Pin 23~26		COM port function	COM port function	COM port function
Pin 21/22,Pin 27/28		EC SPI ROM function	EC SPI ROM function	EC SPI ROM function
PWRGD1/GP13		LAN_RST_L	GP13	S3/S5 GPO High ,S0 GPO Low
PCIRST1#/PCH_D1/GP12		PCI_RST_L	GP12	S3/S5 GPO High ,S0 GPO Low
PCIRST2#/GP11		ECIO_GP11	GP11	GPO High
Pin 36~41		LPC function	LPC function	LPC function
CLKIN_E/KRST#		KBRST_L	Keybaord function	Keybaord function
ESPICLK/PCICLK		CLK_SIO_33M	LPC function	LPC function
PLTRST#/LRESET#		LRST_L_RC	LPC function	LPC function
Pin 48/49/58/59/118/119		SMB_BUS	SMB function	SMB function
Pin 50/51		AMD_TSI	AMD_TSI function	AMD_TSI function
Pin 52/53		BLED_PWM	PWM	PWM function
Pin 54~57		USB function	USB function	USB function
SUSB#/GP45		ECIO_SLP_S3_L_RC	SUSB#	SUSB#
PWRON#/GP44		SIO_PWRON_L	PWRON#	PWRON#
PANSWH#/GP43		FP_PWRBTN_L	PANSWH#	PANSWH#
PSON#/GP42		ATX_PSON_L_R	PSON#	PSON#
SUSC#/GP53		SLP_S5_L_RC	SUSC#	SUSC#
3VBSBW#/GP40/SCL		PM_PCIRST_R	GP40	GPI
Pin 77~80		PS2 function	PS2 function	PS2 function
PCIRST3#/GP10		P80_GPIO	GP10	GPI
RSMRST#/CIRRX1/GP55		RSMRST_L	RSMRST#	RSMRST#
Pin 97		SLP_S3_L	GP93	S3/S5 GPO Low ,S0 GPO High
GP94/ATXPG		ATX_PWRGD	ATXPG	ATXPG
Pin 100		PCIE_RST_L	GP96	GPI
Pin 111~117		LPT function	LPT function	LPT function
Pin 121~Pin128		COM port function	COM port function	COM port function

FCH USB OC Setting

Data:2019/12/03

Function	OC Port	USB 3.0 Port	USB 2.0 Port	Location
OC0# (CPU side)	USB_OC0_L	SS Port 0 SS Port 1	Port 0 Port 1	USB30
OC1# (CPU side)	USB_OC1_L	SS Port 2 SS Port 3	Port 2 Port 3	TYPE C
OC2# (CPU side)	USB_OC2_L	NA	NA	NA
OC3# (CPU side)	USB_OC3_L	NA	NA	NA
OC0# (PM side)	USB_OC0N	SSP Port 0	Port 0	F_USB31_1
OC1# (PM side)	USB_OC1N	SSP Port 1	Port 1	
OC2# (PM side)	USB_OC2N	SS Port 0	Port 2	F_USB30_1
OC3# (PM side)	USB_OC3N	SS Port 1	Port 3	
OC4# (PM side)	USB_OC4N	NA	Port 4	USB_LAN
OC5# (PM side)	USB_OC5N	NA	Port 5	
OC6# (PM side)	USB_OC6N	NA	Port 6	F_USB1
OC7# (PM side)	USB_OC7N	NA	Port 7 Port 8	F_USB2

CPU Strap Setting

Data:2019/03/11

LPC_CLK0_C	
1	BOOT FAIL TIMER ENABLED
* 0	BOOT FAIL TIMER DISABLED

(Type 0 only)

LFRAME_L	
* 1	SPI ROM.(DEFAULT)
0	LPC ROM

(Type 0 and Type 2,4 only)

SYS_RST#	
* 1	normal reset mode(DEFAULT)
0	short reset mode

(Type 0, 1,2,3,4)

LPC_CLK0_C	
0	PSP modify SPI page reg bits [25:24](DEFAULT)
1	PSP not modify SPI page reg bits [25:24]

(Type 4 only)

LPC_CLK1_C	
* 1	Use 48Mhz crystal clock and generate both internal and external clocks.(DEFAULT)
0	Use 100Mhz PCIE clock as reference clock and generate internal clocks only

(Type 0 only)

SPI_CLK_R(ZP)	
* 1	Use 48Mhz crystal clock and generate both internal and external clocks.(DEFAULT)
0	Use 100Mhz PCIE clock as reference clock and generate internal clocks only

(Type 1,2,3,4)

RTC_CLK	
* 1	Coin battery is on board.(DEFAULT)
0	Coin battery is not on board.

(Type 0 only)

AGPIO3	
* 1	Enhanced reset logic(for quicker S5 resume) (DEFAULT)
0	Default to traditional reset logic

(Type 0 only)

FCH Strap Setting

Data:2019/03/11

GPIO_R8 (GPP_G1_SET2)	
UART_TX (GPP_G1_SET1)	
SPI_SDI (GPP_G1_SET0)	
GPP Group 1 (Lanes 7:4)	
* 111	1 PCIe x4
011	1 PCIe x2 + 1 PCIe x2
010	1 PCIe x2 + 2 PCIe x1
001	2 PCIe x1 + 1 PCIe x2
000	4 PCIe x1

(Type 0 only)

GPIO_R4	
* 1	GPP clock source from APU_CLKP/N.
0	GPP / Clock buffer clock source from Crystal

GPIO_R5	
1	USBC SSC disable
* 0	USBC SSC enable

GPIO_R6	
* 1	SATA SSC disable
0	SATA SSC enable

GPIO_R15	
1	PCIe x2 (Lanes 9:8)
* 0	2 PCIe x1 (Lanes 9:8)

PM_DEBUG_EN	
1	Debug mode
* 0	Function mode

GPIO_R7 (GPP_G1_SET2)	
SPI_SDO (GPP_G1_SET1)	
SPI_SCK (GPP_G1_SET0)	
GPP Group 1 (Lanes 3:0)	
111	1 PCIe x4
011	1 PCIe x2 + 1 PCIe x2
010	1 PCIe x2 + 2 PCIe x1
001	2 PCIe x1 + 1 PCIe x2
* 000	4 PCIe x1

(Type 0 only)

TCK (DEBUG_SEL Bit 1)	
TDO (DEBUG_SEL Bit 0)	
* 11	Debug signal group 3 output
10	Debug signal group 2 output
01	Debug signal group 1 output
00	Debug signal group 0 output

REVISION HISTORY:				REVISION HISTORY:				REVISION HISTORY:			
Rev	Date	Page	Notes	Rev	Date	Page	Notes	Rev	Date	Page	Notes
V0.1	2019/12/10		Gerber out	V0.2	2020/2/4	30	Stuff R434 0-04 unstuff R431 for solved USB signal quality issue	V1.0	2020/04/14	7	C550 change from 22P-04 to 33p-04 for fine tune
V0.2	2020/2/5	4	[Follow CRB] M.2 SSD signal change from P565 to CPU	V0.2	2020/1/20	32	DVDD power change from 3V3_S0 to 3V3_S5 for solved 3V3_S0 leakage issue Change power source to 1V8_S0 for vendor suggest Swap comb-hp signal to meet I/O SPEC	V1.0	2020/04/14	8	DEL RJ3 · BIOS can't control EGPIO119 , Board ID detecte by AGPIO18(RJ4)
V0.2	2020/2/4	6	R725 change from 300-04 to 1K-04 , Stuff C772 0.01uF-04 for solved signal quality issue					V1.0	2020/04/14	20	Stuff R297 for not support Modern Standby
V0.2	2020/1/20	7	GPIO change from FCH to APU for solved FCH GPIO_R can't use issue	V0.2	2020/2/4	34	R207,R209 change from 0-04 to 22-04, Stuff C227,C229 47p-04 for solved SMBUS signal quality issue	V1.0	2020/03/23	20	Unstuff R523 for THINK SKU not support Modern Standby
V0.2	2020/2/4	7	[Follow CRB] Connect to AND Gate for PCIE16X reset signal [Follow CRB] Connect to AND Gate for PROM19 reset signal Stuff C471 220P-04 for solved PCIE_RST_L signal quality issue Stuff C550 22P-04 for solved EMI issue	V0.2	2020/1/16	35	Change net SLP_S3_L from GP93 to GP41 for fix G3-S5 Fan turn on isse	V1.0	2020/03/23	20	Unstuff R992 for THINK SKU not support Modern Standby
V0.2	2020/2/5	7	[Follow CRB] M.2 SSD signal change from P565 to CPU	V0.2	2020/2/4	35	R114,R115,R140,R141 change 0-04 to 22-04, Add R1008 22-04 / C1041,C1042,C1043,C1044,C1045 10pF-04 for solved LPC signal quality issue R122,R107 change from 0-04 to 22-04,Stuff C118,C123 47p-04 for solved SMBUS signal quality issue Stuff C120 39P-04 for solved LPC_RST signal quality issue R1,R2 change from 0-04 to 22-04 , Stuff C1,C2 47p-04 for solved SMBUS signal quality issue Add C1049 0.1uF-04 for solved PSON# signal quality issue	V1.0	2020/03/23	20	Stuff R182,R170,R165 for THINK SKU not support Modern Standby
V0.2	2020/1/16	8	Add C1016 1000pF for fix auto reset issue					V1.0	2020/04/14	26	ADD R1040 100K-04 let USB_EN power down faster
V0.2	2020/1/20	8	Net change from FCH to APU for fix FCH GPIO_R can't use issue	V0.2	2020/2/4	35	ADD C1055 150uF-04 for solved SLP_S3_L signal quality issue	V1.0	2020/04/14	35	ADD GP15(ECIO Side) control S03/S3 power
V0.2	2020/2/5	8	[Follow CRB] M.2 SSD signal change from P565 to CPU	V0.2	2020/2/4	36	LED Power source change from +5V_S5 to +5V_S0 for G3-S5 LED turn on issue	V1.0	2020/04/14	45	R418 change from 10K-04 to 20K-04 for fine tune
V0.2	2020/2/4	8	Stuff C418 to 10p-04 , C417,C394,C388 to 22p-04 ,C426 to 22pF-04, R399 to 10-04 for solved SPI signal quality issue	V0.2	2020/2/4	38	ADD QN24,R1010,C1048 for solved TPM_RST signal quality issue	V1.0	2020/04/14	47	Unstuff R999,R998,R995,Q52,R489,Q51,C1017,Q53 ADD R1039 Use GP15(ECIO Side) control S03/S3 power
V0.2	2020/1/31	9	Unstuff [Del] SC39,SC40,SC42,SC83,SC115,SC119 22U-6V3X5 Add 47U-6V3X5-08 / SC39,SC40 [2pcs] place on SOCKET Bottom For SDLE test , NB_VCORE Transient fine tune Un-Stuff / Del [22U-6V3X5] C678,C677,C684,C685,C689,C687 [4pcs] [CPU Socket Top] Add [47U-6V3X5-08] C678,C677,C684,C685 [4pcs] [CPU Socket Top] For SDLE test , NB_VCORE Transient fine tune Del SC70,SC46,SC52,SC56,SC71,SC63,SC64,SC65,SC72,SC57,SC69,SC73,SC78 [13pcs] Add Reserve SC42,SC46,SC52,SC57 [4pcs] 22U-6V3X5-X-0 Reserve place 22U-6V3X5 spacing for NB_VCORE SDLE test fine tune Un-Stuff [22U-6V3X5] C878,C880,C893,C902,C910,C918,C921,C879,C920,C913,C907,C900,C890,C891,C888,C839,C846 [17pcs] [CPU Edge right side] For SDLE test , NB_VCORE Transient fine tune	V0.2	2020/2/6	39	R300 change from 3V3_S5 to 3V3_S0 for solved PM_PWRGD signal quality issue R281 change from 10K-04 to 100K-04 for solved PM_PWRGD signal quality issue	V1.0	2020/04/14	47	Unstuff R180 ,ADD LPC_SMI control circuit follow CRB
V0.2	2020/2/4	11	R384,R391 change from 0-04 to 22-04, Stuff C431,C439 47p-04 for solved SMBUS signal quality issue ADD C1047 0.01U-04 for solved DRAMRST_A signal quality issue	V0.2	2020/2/4	40	Change BAT1 Footprint to use correct package	V1.0	2020/04/14	47	U9.update footprint.
V0.2	2020/2/4	12	Stuff C743 0.01U-04 for solved DRAMRST_B signal quality issue	V0.2	2020/1/31	41	C956 change from 330p to 470p For SDLE test VCCORE comp fine tune R864 change from 53.6K-1-04 to 68K-1-04 For SDLE test VCCORE LL fine tune C923 change from 330p to 470pF For SDLE test NBVCORE comp fine tune Modify R890 [2.2-08] tie From +5V_S0 To +5V_S5 Reserve R990 [2.2-06] tie +5V_S0 Improve S0 +5V_S0 leakage Improve R+12V_4Pin modity to S0 , Eup current	V1.0	2020/04/14	48	R749 change from 13Kto 13.3K
V0.2	2020/1/16	13	Change R782,R797,R800,R801,R805,R819,R826,R837 from 470R to 499R for follow AMD schematic checklist Add R990,R991 pull-hi 2.2k resistor for HDMI function	V0.2	2020/1/31	42	Unstuff EC34 820uF/2.5V OS60N Add SPC2 ETPC820uX3B [place on Socket Bottom] For SDLE test NBVCORE transient fine tune	V1.0	2020/04/17	48	L7 update footprint [the same as L14]
V0.2	2020/2/4	13	ADD R1012,C1050 for solved DP_AUXN signal issue	V0.2	2020/1/31	43	Modify Q9 From 3904 BJT To 7002 MOS For SLP_S3_L signal division voltage issue	V1.0	2020/04/17	18	Stuff R275 follow CRB
V0.2	2020/1/16	14	Change R732,R734,R728,R721,R709,R717,R797,R743 from 470R to 499R for follow AMD schematic checklist	V0.2	2020/2/3	43	Reserve Pull Hi Resistor tie 12V_SB power rail Change Pull Hi Power source from 5V_S5 to 12V_SB power rail Modify R367 to 200K / C395 to 1uF for solve Renoir can't power on issue				
V0.2	2020/2/4	14	ADD R1013,C1051 for solved HDMI SDA signal quality issue	V0.2	2020/1/31	44	Reserve [10U-16VX5-08] C689,C1035 [2pcs] For +1V2_DIMM Vin RMS (FB R613 need modity routing From EC22) Improve +1V2_DIMM Jitter Modify C634 From .01U-25VX7-04 To 4700P-25VX7-04 Modify R613 From 100-1-04 To 0-04 Improve +1V2_DIMM Jitter / Power Noise Stuff R780 From 10K-04-0 To 0-04 And Modify R780 tie From +3V3_S5 To +5V_S5 Improve +5V_VTT LDO Vout [Add RCR] Modify R778 (SLP_S3_L) From Tie USB Vout To USB Pin3 REFEN Pin For +DDR_VTT S3 Power off Modify C800 From 1U-16VX7 To .1U-16VX7-04 Stuff EC28 To 820U-2V5LD6H9E Modify DDR_VTT Feedback [2ms] and Improve Droop Change PFB11 to 0 ohm [Short Pad] Improve Jitter Add [22U-6V3X5] C1034 [1pcs] Improve Jitter				
V0.2	2020/1/16	16	Change U46 IT6516BPN/CX from 0068(R) to 0076(R) for Fix VGA Display issue	V0.2	2020/1/31	45	Modify C259,C260 [2pcs] From 10U-6V3X5 To 22U-6V3X5 Improve SDLE Test +VDDP_S0 Heavy Load drop				
V0.2	2020/2/4	17	Add MOS Q54,R1009 to solved voltage too low issue	V0.2	2020/2/3	46	Change +VDD_FCH power source/enable to S5 power for Modern standby function use Reserve FCH Power Gate for modern standby function use				
V0.2	2020/1/16	18	Change R181 from 200k to 10k for follow AMD CRB (Artic)	V0.2	2020/2/3	47	Reserve FCH Power Gate for modern standby function use Change +2V5_FCH power source/enable to S5 power for Modern standby function use				
V0.2	2020/2/4	18	[Follow CRB] Connect to AND Gate for PROM19 reset signal Reserve PROM19 reset signal from ECIO or CPU side.	V0.2	2020/1/20	20	Reserve FCH Power Gate for modern standby function use				
V0.2	2020/1/20	20	Reserve FCH Power Gate for modern standby function use								
V0.2	2020/2/4	21	R305,R310 change from 0-04 to 22-04, Stuff C321,C323 47p-04 for solved SMBUS signal quality issue R157,R159 change from 0-04 to 22-04, Stuff C156,C163 47p-04 for solved SMBUS signal quality issue								
V0.2	2020/2/4	22	R108,R117 change from 0-04 to 22-04, Stuff C129,C133 47p-04 for solved SMBUS signal quality issue Stuff R147 22-04,C148 22P-04 for solved PCICLK signal quality issue								
V0.2	2020/2/4	23	R48,R49 change from 0-04 to 22-04, ADD C1052,C1053 47p-04 for solved SMBUS signal quality issue Stuff C68 220P-04 for solved WLAN_RST_L signal quality issue								
V0.2	2020/2/4	24	Stuff C77 330P-04 for solved SSD_RST_L signal quality issue								
V0.2	2020/2/5	24	[Follow CRB] M.2 SSD signal change from P565 to CPU								